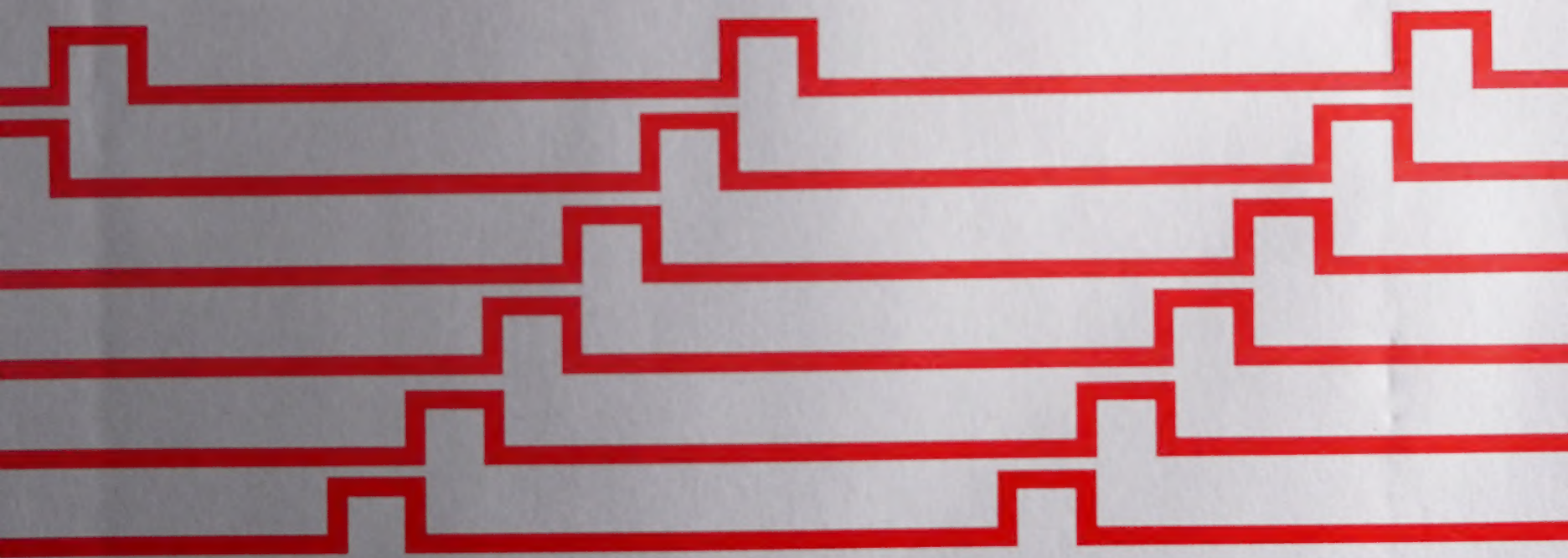
Gould Biomation K101-D/K102-D Logic Analyzers

Service Manual



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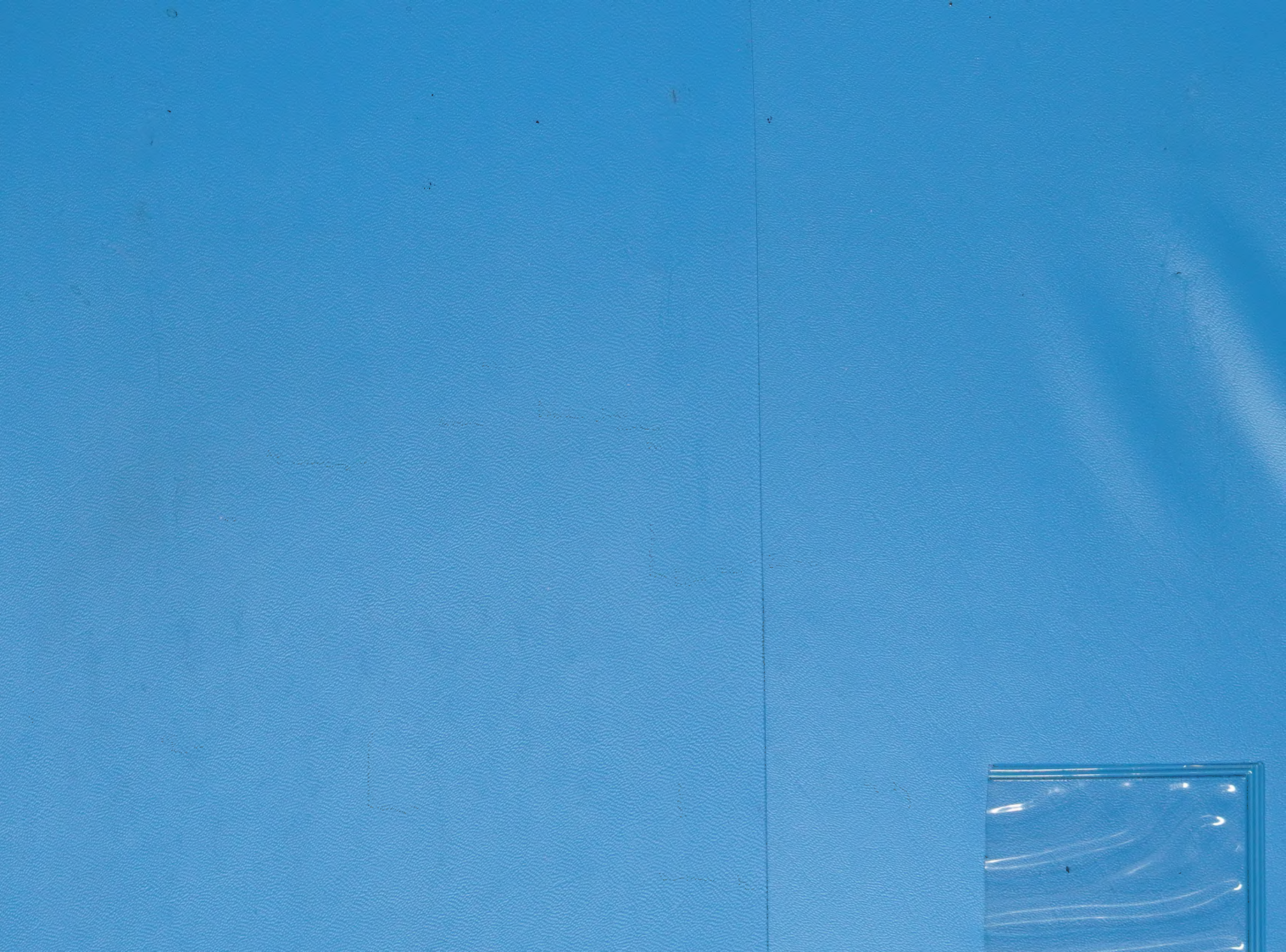
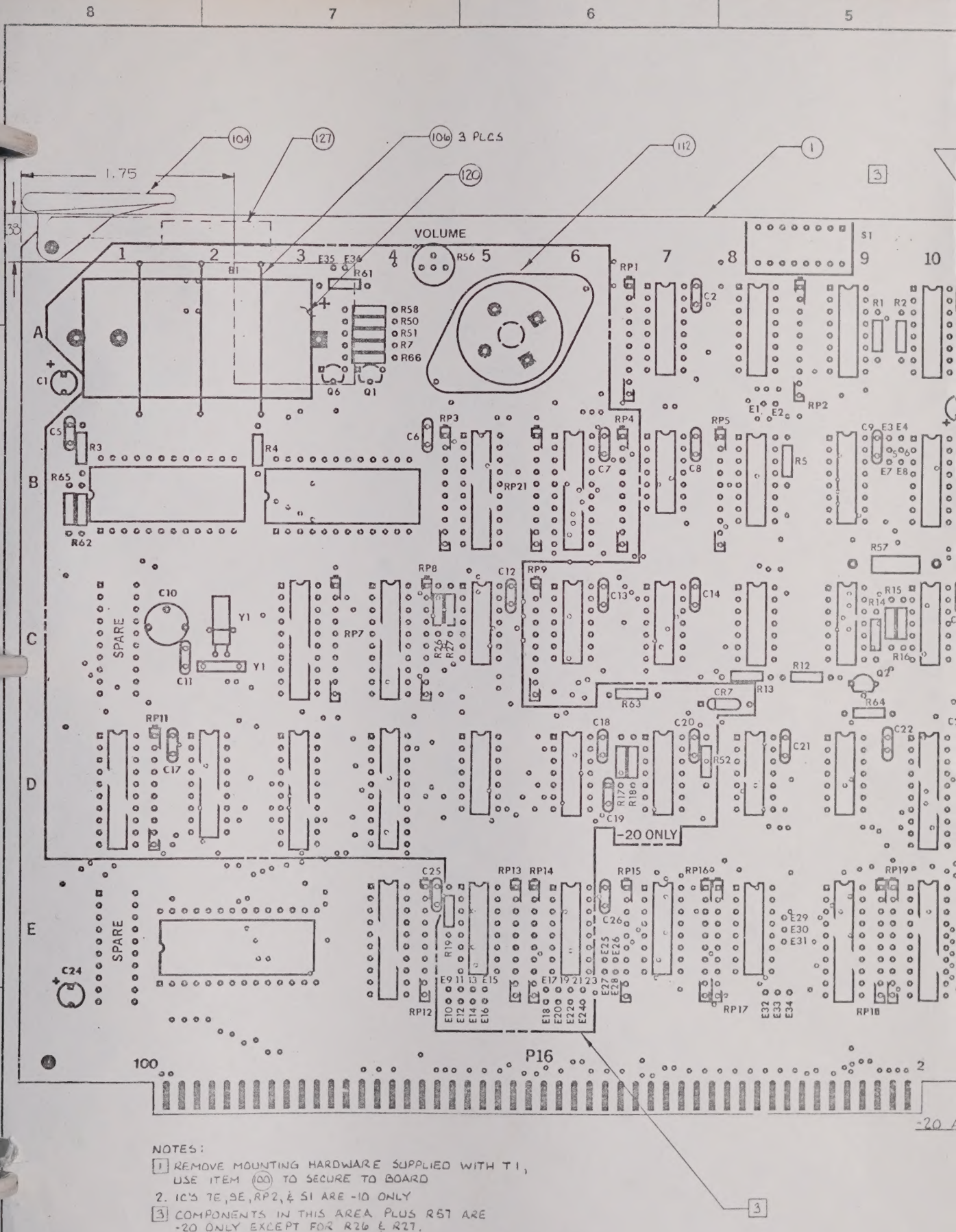
Electronics & Electrical Products





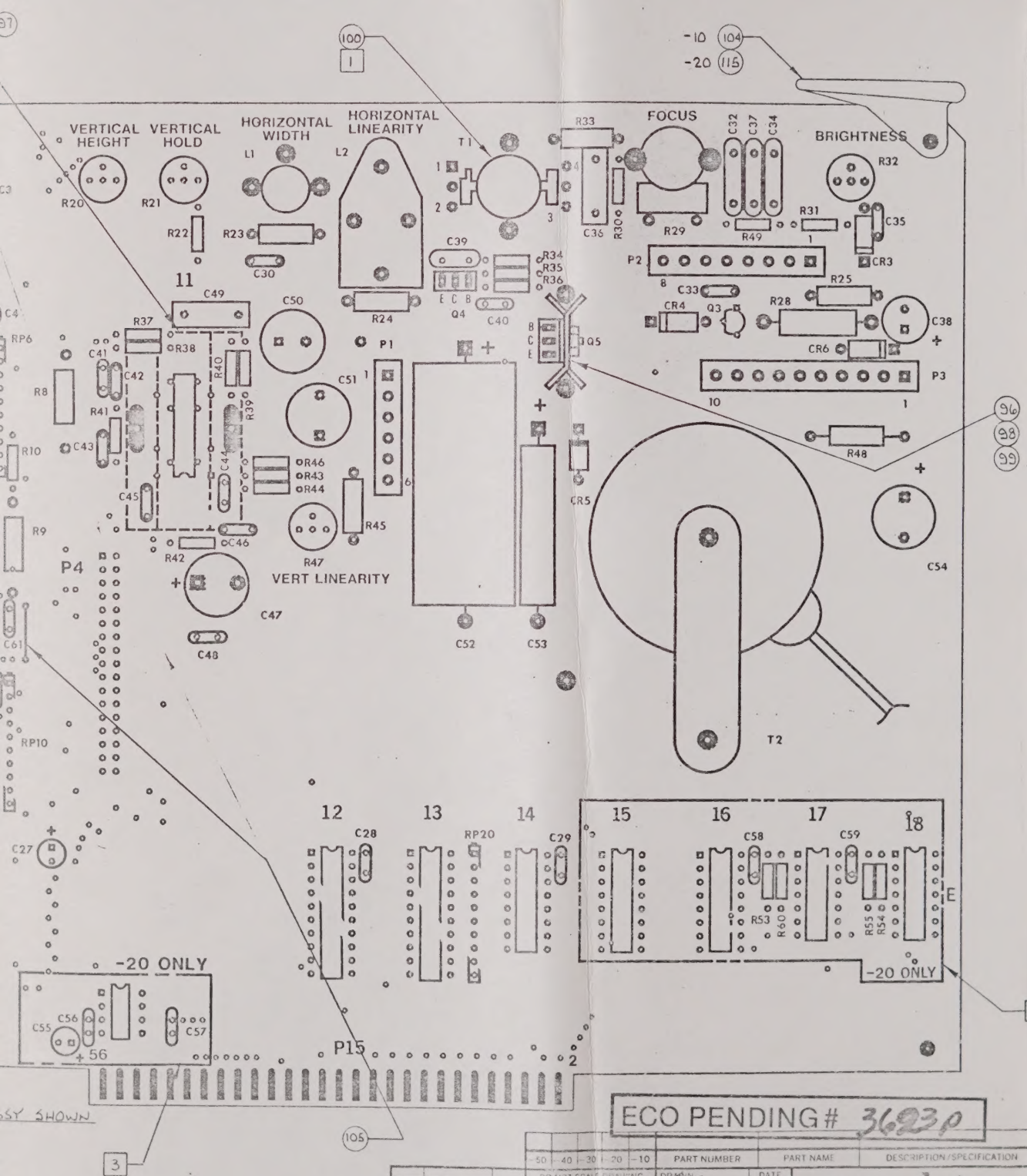
NOTES:

1. REMOVE MOUNTING HARDWARE SUPPLIED WITH T1, USE ITEM (100) TO SECURE TO BOARD
2. IC'S 7E, 9E, RP2, & S1 ARE -10 ONLY
3. COMPONENTS IN THIS AREA PLUS R57 ARE -20 ONLY EXCEPT FOR R26 & R27.

DWG. NO.	SH	REV
0114-0190	2	U

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CK
			SEE SHT 1		



ECO PENDING # 3623P

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0.599 ± .002; 1.000 1.499 ± .005

DASH NO	NUMBER	QTY
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

ENG. SERV | DATE

DRAWN: S. RIDELL | DATE: 5-12-81

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomatic

TITLE: ASSEMBLY, DATA DISPLAY BOARD

SCALE | SIZE: D | PART NUMBER: 0114-0190

CODE: K101/K500 | SHEET 2

JUMPER	AS ETCHED	-20 K101	-10 K500	DESCRIPTION
E1 TO E2	OUT		JUMPER FOR 50HZ ONLY	CRT SCAN RATE IN=50HZ. OUT=60HZ
E3 TO E4	OUT			NOT USED
E5 TO E6	OUT			NOT USED
E7 TO E8	OUT		JUMPER	IN = K500 HORIZ. SCAN OUT=K101
E9 TO E10	IN			A18 }
E11 TO E12	OUT			A17 }
E13 TO E14	IN			A16 }
E15 TO E16	IN			A15 } K101 CMOS RAM
E17 TO E18	IN			A14 } ADDRESS SELECTION
E19 TO E20	IN			A13 }
E21 TO E22	IN			A12 }
E23 TO E24	IN			A19 }
E25 TO E26	IN			A8 } K500 MEM MAPPED I/O
E27 TO E28	IN			A7 } ADDRESS DECODE
E29 TO E30	IN		CUT	IN SELECTS I/O MAPPED I/O (K101)
E30 TO E31	OUT		JUMPER	IN SELECTS MEM MAPPED I/O (K500)
E32 TO E33	IN		CUT	IN FOR K101
E33 TO E34	OUT		JUMPER	IN FOR K500

4 | 3 | DWG. NO. 0114-0190 | SH 1 | REV U | 1

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	R	2462	REVISED PER ECO	[illegible]	[illegible]	5/19/82
	S	2509	REVISED PER ECO *	George	[illegible]	[illegible]
	T	2601	REVISED PER ECO *	George	[illegible]	
	U	2635	REVISED PER ECO *	George	[illegible]	

ECO PENDING # 3623p

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO	NUMBER	QTY
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0.599 ± .003; 1.000 ± .999 ± .004; 1.000 ± .999 ± .005

ENG. SERV. | DATE

DRAWN: DWUGE | DATE: 3/25/82

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY DATA DISPLAY BD

SCALE	SIZE	PART NUMBER	REV
2/1	D	0114-0190	U

CODE K101/K500 | SHEET 1 OF 2

K101 K500

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART
1					1	1	0114-
2					3	2	3000
3					1	1	3000
4					2	2	3050
5					1	1	3000
6					2	2	
7					12	2	
8					4	—	
9					1	1	
10					2	2	
11					2	2	
12					1	1	
13					2	1	
14					1	1	
15					1	1	
16					—	1	
17					2	2	3000
18					1	1	3050

COMMENTS		TOTAL COST	UNIT COST
[1] USED ON -20 ONLY			
[2] USED ON -10 ONLY			
-10 K500			
-20 K101			

ASSEMBLY TIME

COMPONENT LEAD SPACING
1/4W RES - .40
1/8W RES - .40
1/2W RES - .50
1W RES - .70

ECO PENDING # 3623

DASH NO.	NUMBER	QTY
-20	0114-0002	1
-10	0950-0002	1
	NEXT ASSEMBLY	

DRAWN	J. WEL
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURAN	

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
0192	PWB				FAB
-2000	RESISTOR	R35, 36 [1] R64		200Ω, 1/4W, 5%	
-3307	RESISTOR	R38		3.3Ω, 1/4W, 5%	
-4700		R8,9		470Ω, 1/2W, 5%	
-8206		R12		82Ω, 1/4W, 5%	
-4700		R5, 34		470Ω	
-2201		[2] R1, 2 [1] R19, 1, 2, 53-55, 58, 3, 4, 60, 62, 65		2.2K	
-1002		R17, 18, 52, 63		10K	
-5601		R46		5.6K	
-8201		R39, 40		8.2K	
-4702		R43, 44		47K	
-1203		R22		120K	
-2203		R41 [1] R37		220K	
-2703		[2] R37 [1] R42		270K	
-5103		R31		510K	
-6803		R42		680K	
-1004	RESISTOR	R30, 49		1MEGΩ, 1/4W, 5%	
-2200	RESISTOR	R24		220Ω, 1/2W, 5%	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PROTO REL	8-1-80	J.W.		
	B	updated prototypes ET-HA		CB		
	C	PROTOTYPE	11-26-80	R.H.		
	D	PILOT RELEASE PER ERN # 0091	12-22-80	N.B.	RD	
	E	REVISED PER ECO # 1539	3-21-81	MS	JL	
	F	REVISED PER ECO # 1512	3-21-81	MS	JL	
	G	REVISED PER ECO # 1653	5-28-81	SR	JL	

DON | DATE 8-1-80

CE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-0190 | REV 4

MODEL K101/K500 | CODE | SHEET 1 OF 8

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART
19					1	1	3050
20					2	1	3050
21					1	1	3050
22					1	1	SELEC TES
23							
24					1	1	320C
25					1	1	307C
26					1	1	310C
27					1	1	310C
28					1	1	310C
29					1	1	310C
30					1	1	3300
31					3	3	3300
32					1	1	3300
33					1	1	4100
34					1	1	4100
35					8	6	400C
36					5	4	440C
							REF

			DRAWN J. WEB
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURAN
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-1007	RESISTOR	R45		1.0 Ω, 1/2W, 5%	
-3906	↑	R25 [1] R57		39Ω, 1/2W, 5%	
-1000		R33		100Ω, 1/2W, 5%	
TED AT T		R23		S.A.T.	
-0008		R48		1.0 Ω, 1W, 3%	
-1501		R28		1.5 KΩ, 1W, 5%	
-7500		R13		75 Ω, 1/8W, 1%	
-6040		R14		604 ↑ ↑	
-8250	↓	R15		825 ↓ ↓	
-9090	RESISTOR	R16		909 Ω, 1/8W, 1%	
-0084	RES. VAR.	R47		50K	
-0085	↑	R20,21,32		100K	
-0088	RES. VAR.	R29		1MEG	
-0024	CAPACITOR	C43		68 PF, 500V MKA	
-0002	↑	C39		470PF, 500V MICA	
-0009		C33,35,42,44-46 [1] C5,6,		0.1MF, 100V	
-0043	CAPACITOR	C1,C4,C24,C27 [1] C19		47 MF, 6V	

F. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	H	REVISED PER ECO # 1693	5-28-81	SR	JL	
	J	REVISED PER ECO # 1694	6-1-81	SR	JL	
	K	REVISED PER ECO # 1803	6-11-81	SR	JL	
	K	PROD RELEASED PER ERN # 0129	6-11-81	SR	JL	
	L	REVISED PER ECO # 1955	9-11-81	TM	BD	
	M	REVISED PER ECO # 2043	10-9-81	TM	BD	
	N	REVISED PER ECO # 2075	10/28/81	RL	BD	

DON	DATE 7-31-80
ICE	

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-0190 | REV U

MODEL K101/K500 | CODE | SHEET 2 OF 8

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PAR
37					2	2	400
38					—	1	440
39					3	3	400
40					26	17	401
41					1	—	401
42					1	1	440
43					2	2	440
44					1	—	440
45					1	1	420
46					1	1	440
47					1	—	700
48					1	1	120
49					3	3	1200
50					1	1	430
51					1	—	300
52					1	1	610
53					1	1	SELE TE
54					1	—	460
							R

			DRAWN J.WE
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0042	CAPACITOR	C36,49		.15μF, 100V	
-0039		C55		10μf / 16V	
-0045		C32,34,37		.01μF, 500V	
-0103		C40,41,2,3,8,9,13,14,16,21-23,25,26,28,29,48 [1] C7,12,17,19,30,5',57,58,59		.01μF, 50V	
-0100		C11		10pf, 100V	
-0036		C51		1000μF, 16V	
-0037		C47,54		470μF, 25V	
-0047		C50		220μF, 35V	
-0036-10	CAPACITOR	C52		6μF, 200V	
-0038	CAPACITOR	C38		10μf, 100V	
-0451	BATTERY	B1	POWER CONV. INC.	2.4V NICD	
-0033	DIODE	CR5	3SF4		
-0031	DIODE	CR3,4,6	IN4937		
-0041	CAPACITOR	C53		.056μf, 400V	
-0100	RESISTOR	R66		390Ω, 1/4W, 5%	
-0151	SOCKET	X2E		28 PIN	
CTED AT	CAPACITOR	C30		S.A.T.	
-0010	CAP, VAR	C10		7-40 pf	

REVISIONS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	P	REVISED PER ECO # 2173	[illegible]	[illegible]	RD	
	Q	REVISED PER ECO # 2132	[illegible]	[illegible]	RD	
	R	REVISED PER ECO # 2462	[illegible]	[illegible]	[illegible]	
	S	REVISED PER ECO # 2509	6-25-82	[illegible]	GW	
	T	REVISED PER ECO # 2601	6-25-82	[illegible]	GW	
	U	REVISED PER ECO # 2635	6-25-82	[illegible]	GW 10-26-82	

LDSN	DATE 7-31-82
ANCE	

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

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B	0114-0190	REV U

MODEL K101/K500 | CODE | SHEET 3 OF 8

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART
55					2	1	1300
56					1	–	1400
57					1	1	1300
58					1	1	1300
59					2	3	6100
60					1	–	3000
61					–	1	0950
62					8	8	3700
63					5	–	3700
64					7	5	3700
65					1	1	1500
66					1	1	1800
67					1	1	1800
68					2	1	
69					1	1	
70					2	1	
71					2	1	
72					1	1	1800
							REF

			DRAWN J. WE
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0008	TRANSISTOR	Q2 [1] Q6	2N3904		
-0019	↑	Q1	2N3906		
-0049	↓	Q5	BVL07		
-0048	TRANSISTOR	Q4	2N4921		
-0120	SOCKET	X8S, X10B, X5I [1] X8S, X10B		16 PIN	
-6300	RESISTOR	R51		680Ω, 1/4W, 5%	
-0195	IC	10B		PROM, HORIZ	
-0083	RESISTOR PACK	RP1,5,6,9,12,15,20, [2] RP2 [1] RP14		2.2KΩ, 10 PIN SIP	
-0085	↕	RP 3,7,8,11,21		22KΩ 10 PIN SIP	
-0049	RESISTOR PACK	RP 10, 16-19 [1] RP 4,13		3K/6.2KΩ 10PIN SIP	
-0018	TRANSISTOR	Q3		VN10KM	
-0105	I.C.	7C	74LS00		
-0123	↑	6C	74LS14		
-0110		9D [1] 9D, 5D	74LS10		
-0111		8D	74LS20		
-0115		7B [1] 17E	74LS74		
-0254	↓	[2] 17E [1] 5E, 6E	74LS85		
-0117	I. C.	9C	74LS86		

ENGG	REV	DESCRIPTION	DATE	DWN	CKD	APP'D

DSGN	DATE 8-1-80
NCE	
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LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B	0114-0190	REV U

MODEL K101/K500 | CODE | SHEET 4 OF 8

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PART
	-60	-50	-40	-30	-20	-10	
73					1	1	1800
74					6	6	1
75					1	1	
76					3	2	
77					3	2	
78					3	1	
79					3	1	
80					1	1	
81					2	1	
82					1	1	1800
83					1	—	0114
84					2	—	1826
85					1	1	1800
86					1	—	0114
87					1	1	1700
88					1	—	1800
89					1	—	1800
90					—	1	0950

			DRAWN J.W
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0301	I. C.	14E	74LS156		
-0125		7A-10A [1] 15E,16E	74LS161		
-0121		9B	74LS175		
-0227		10D, 4E[illegible] [1] 6B, 4E, 10D	74LS240		
-0240		13E, [2] 9E [1] 5B, 1D	74LS244		
-0268		10E [1] 3C, 4C	74LS245		
-0231		12E [1] 3D 4D	74LS273		
-0193		8E	74LS138		
-0097		10C [1] 18E	7406		
-0038		8C	74S20		
-0064		8B		PROM, VERTICAL	
-0080		1B, 3B	6116LP-3		
-0319		2E	8259-A		
-0065		10B		PROM, HORIZONTAL	
-0082		11B	TDA-1270	VERTICAL PROCESSOR	
-0341		2D	MSM5832		
-0311	I.C.	7D	7438		
-0194	I.C.	8B		PROM, VERT	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

LDON	DATE 8-1-80

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B 0114-0190 REV U

MODEL K101/K500 CODE SHEET 5 OF 8

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -00	-50	-40	-30	-20	-10	PAR
91					1	1	900
92					1	1	015
93					1	—	510
94					1	1	013
95					1	1	900
96					1	1	700
97					1	1	700
98					1	1	700
99					1	1	720
100					1	1	2400
101					1	1	6000
102					1	1	6000
103					1	1	6000
104					1	2	700
105					2	2	900
106					3	—	720
107					—	1	660
108					1	1	300
							R

			DRAWN J. WE
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
0-0049	COIL ASSY, WITH	L1		5-	
-0011	COIL ASSY, LIN	L2			
-0012	CRYSTAL	Y1		32.768	
-0014	TRANSFORMER	T1			
-0082	TRANSFORMER	T2		FLYBACK	
-0305	HEATSINK	@Q5			
-0366	HEATSINK	@11B			
-0221	INS. WASH	@Q5			
-0017	INSULATOR	@Q5			
-0004	MTG BRACKET	@T1			
-0359-6	HEADER	P1		6PIN	
-0359-8	↕	P2		8PIN	
-0359-10	HEADER	P3		10PIN	
-0120	EJECTOR				
-0094	GND WIRE				
-0032	MOUSE TAIL			.115 DIA, 4"	
-0037	DIP SWITCH	S1			
-1001	RESISTOR	R10		1K, 1/4W, 5%	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN DATE 8-1-80

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-0190 | REV U

MODEL K101/K500 | CODE | SHEET 6 OF 8

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART
109					1	1	300
110					1	1	300
111					1	—	330
112					1	—	740
113					1	—	170
114					1	—	440
115					1	—	0112
116					1	—	180
117					1	—	180
118					1	—	300
119					1	—	100
120					A/R	—	830
121					1	—	400
122					1	—	600
123					1	—	6100
124					2	—	6100
125					1	—	300
126					1	—	300

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	J. WEI
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSUR	

RT NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
0-2200	RESISTOR	R26		220Ω, 1/4W, 5%	
-3300	RESISTOR	R27		330Ω, 1/4W, 5%	
0-0056	RES., VAR.	R56		1K, 1 TURN	
-0002	BEEPER				
0-0071	I.C.	11C		LF356	
0-0045	CAPACITOR	C55		33μf, 25v	
0228-08	EJECTOR, STAMPED			"A8"	
0-0351	I.C.	5C		74LS12	
0-0352	I.C.	6D		74LS22	
-5106	RESISTOR	R61		51Ω, 1/4W. 5%	
-0032	DIODE	CR7		IN4152	
-0027	INSULATION	3M4108		1"x 1" x 1/8" THK	
-0011	CAPACITOR	C61		2.2 μf	
0-0389	HEADER	P4		34 PIN - FLOPPY	
-0146	SOCKET	2D		18 PIN	
-0122	SOCKET	1B. 3B		24 PIN	
0-2700	RESISTOR	R7		270Ω, 1/4W, 5%	
0-3301	RESISTOR	R50		3.3K. 1/4W. 5%	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DWN | DATE 8-1-80

LIST OF MATERIAL

DATA DISPLAY
PWB ASSY

biomation

B | 0114-0190 | REV U

MODEL K101/K500 | CODE | SHEET 7 OF 8

ITEM	QUANTITY PER ASSEMBLY									PART NUMBER	PART NAME
	-50	-40	-30	-25	-20	-15	-12	-10	-7		
127								1	—	0114-043E	LABEL, CAUT

NOTES

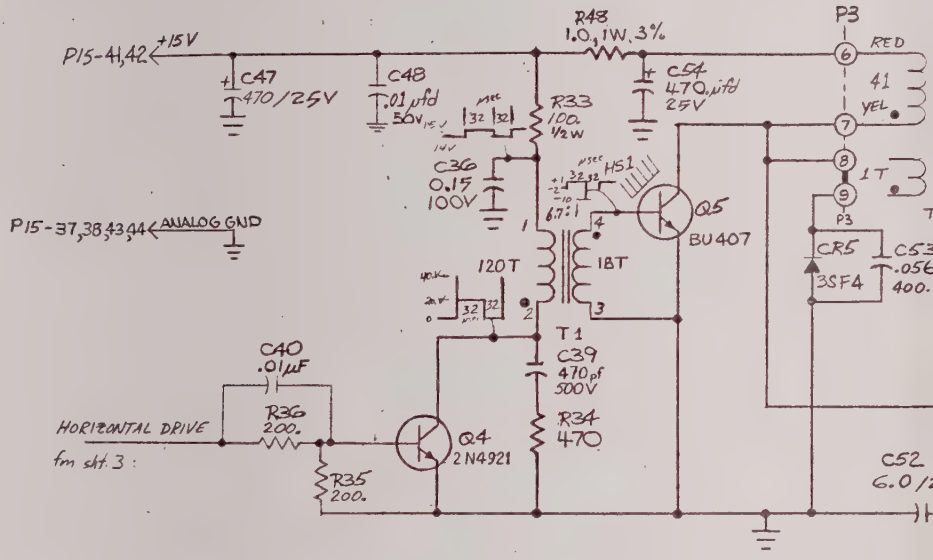
/ DESCRIPTION	REFERENCE DESIGNATION	L/M
ION NICD ONLY!		

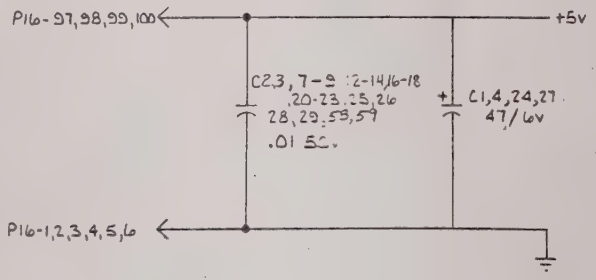
LIST OF MATERIAL

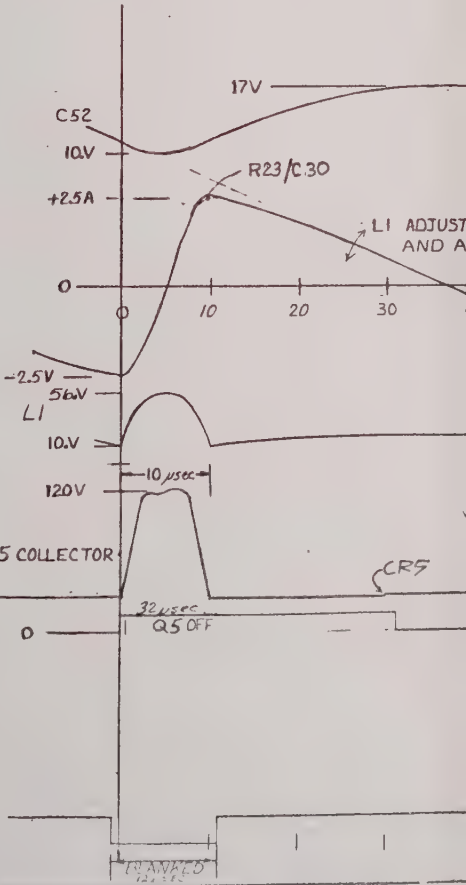
DATA DISPLAY PWA ASSY

GOULD biomation

B	0114-0190	REV U
MODEL K101 / K500	SHEET 8 OF 8	





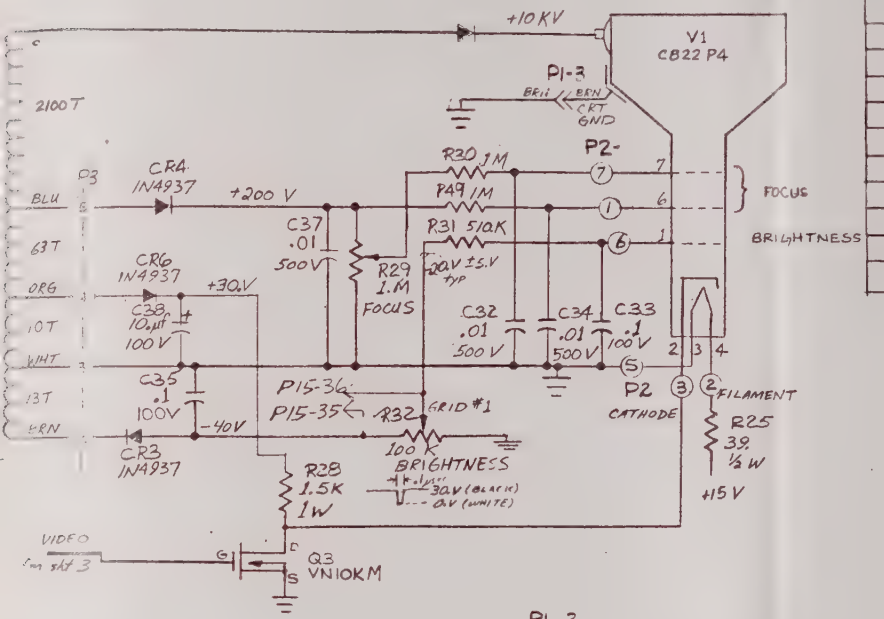


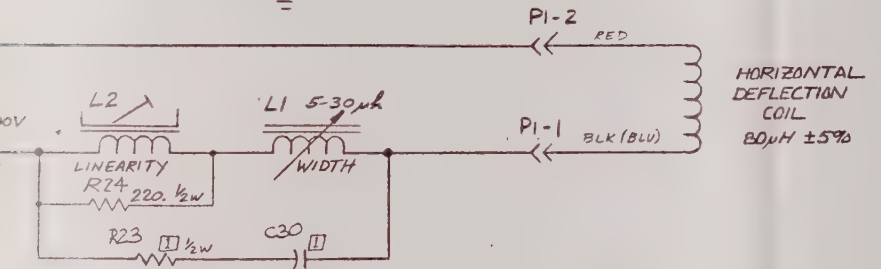
NOTES

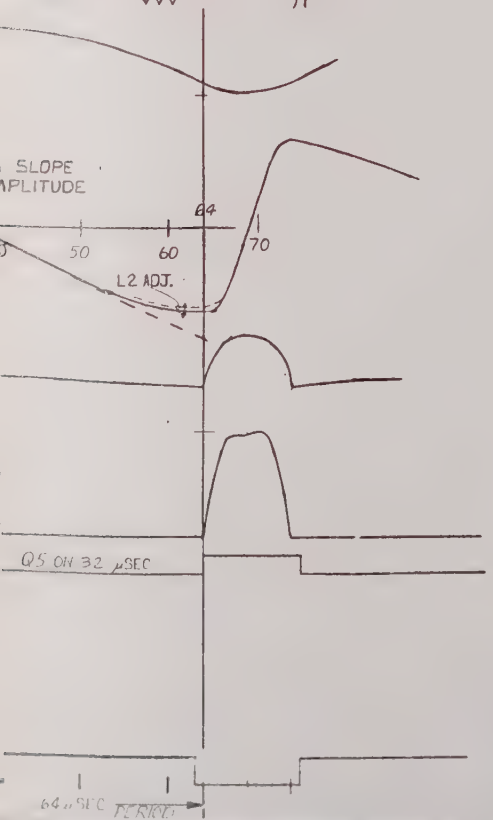
1. SELECTED AT TEST. NOT NORMALLY USED. R23 = 100Ω C30 = .002 µF MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ LINEARITY AT LEFT SIDE OF DISPLAY
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. -10 ONLY

DWG NO 0114-0191 | SH 1 | REV F

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	--	ADD SHTS 3,4,5 SCHEMATIC + CMOS RAM	[illegible]		2-20-7[illegible]
	B	—	prototype update to ETCHA	[illegible]		10-5-81
	C	—	update to ETCHB added clock redraw [illegible]	[illegible]		10-8-81
	D		REVISED PILOT RELEASE ERN# [illegible]	[illegible]	RG	11-8-81
	D	—	PROD REL ERN #0129	[illegible]	RG	4-9-81
	E	1693	REVISED PER ECO	[illegible]	JL	6-1-81
	F	1694	REVISED PER ECO	[illegible]	JL	6-1-81
	G	1955	REVISED PER ECO	[illegible]	RD	10-15
	H	2043	REVISED PER ECO	[illegible]	RD	10-15
	J	2123	REVISED PER ECO	[illegible]	RD	11/18/81
	K	2462	REVISED PER ECO	[illegible]	[illegible]	5/[illegible]
	L	2601	REVISED PER ECO	[illegible]	[illegible]	
	M	2635	REVISED PER ECO	[illegible]	[illegible]	
	N	2704	REVISED PER ECO	[illegible]	[illegible]	
	P	3500	" " " N°	DGW	1-27-[illegible]	[illegible]







ECO PENDING # 3623 P

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: 0.599 ± .001, 500.999 ± .004, 1.000 1.499 ± .005

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV | DATE

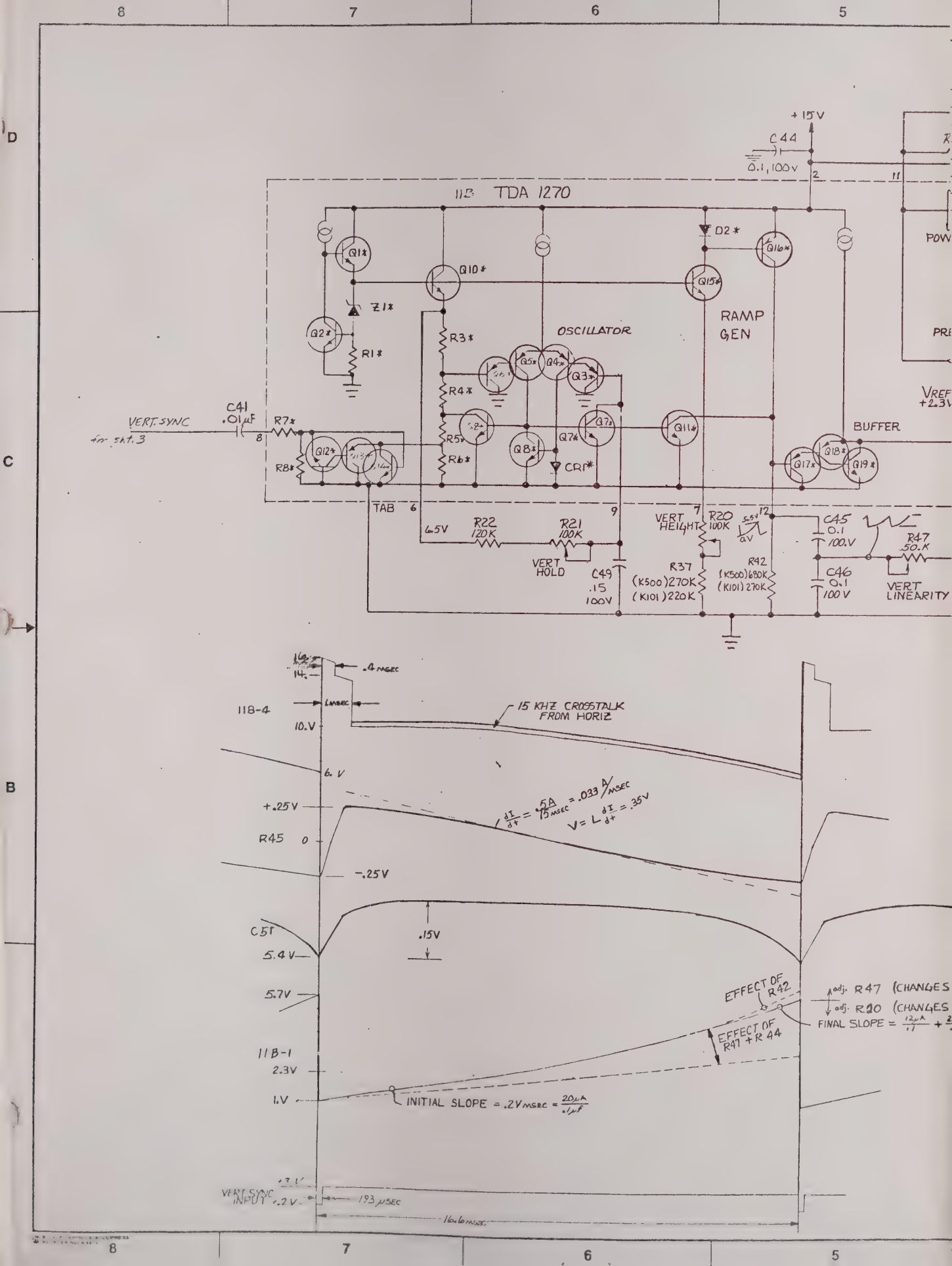
DRAWN	[illegible]	DATE 6-25-80
CHECKED	[illegible]	1-14-81
PROJ ENG	[illegible]	1-14-81
MANUFACTURING		
QUALITY ASSUR		

GOULD biomation

TITLE SCHEMATIC DATA DISPLAY PWB

SCALE	SIZE	PART NUMBER	REV
	D	0114-0191	P

CODE [illegible] | SHEET 1 OF 6

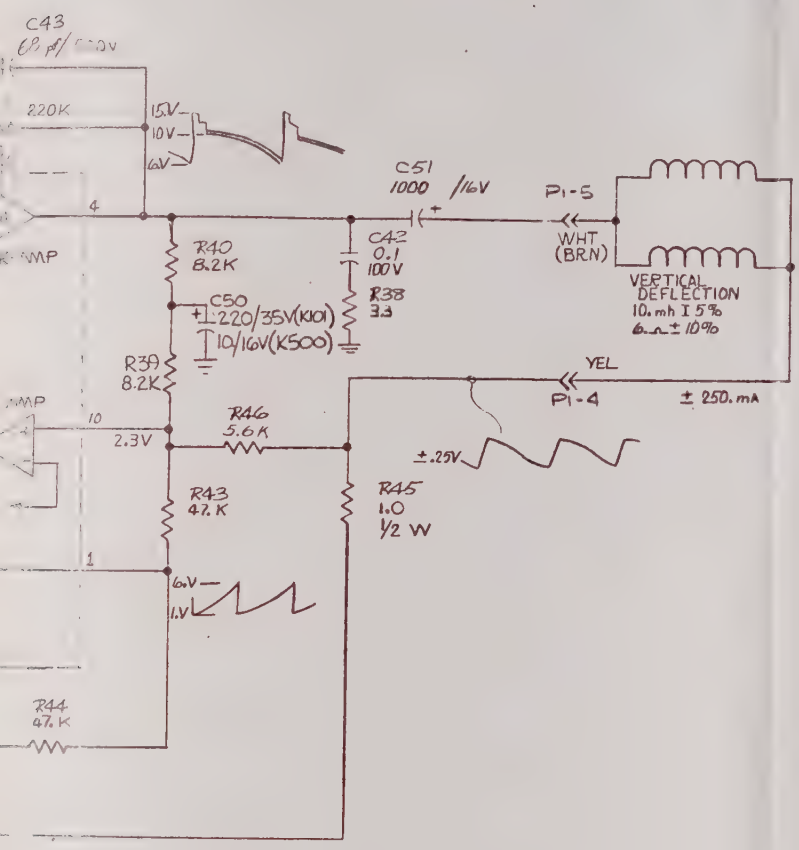


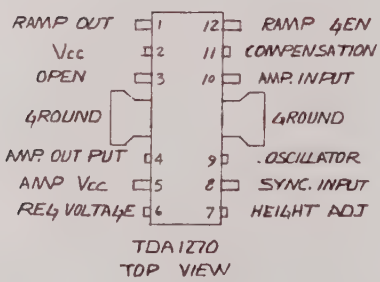
+15V
C44
0.1, 100V
11B TDA 1270
D2*
Q1*
Q10*
Q16*
Q15*
Z1*
Q2*
R1*
R3*
OSCILLATOR
RAMP GEN
Q5*
Q4*
Q3*
R4*
VERT. SYNC
for sht. 3
C41
.01µF
R7*
R8*
Q12*
R5*
R6*
Q8*
Q7*
Q11*
CR1*
BUFFER
Q17*
Q18*
Q19*
TAB
6.5V
R22
120K
R21
100K
VERT HOLD
C49
.15
100V
VERT HEIGHT
R20
100K
R37
(K500)270K
(K101)220K
R42
(K500)680K
(K101)270K
C45
0.1
100.V
C46
0.1
100V
R47
50.K
VERT LINEARITY
POW
PRE
VREF
+2.3V
.4 MSEC
1 MSEC
11B-4
10.V
15 KHZ CROSSTALK FROM HORIZ
6. V
+.25V
R45
0
-.25V
dI/dt = .5A/15 MSEC = .033 A/MSEC
V = L dI/dt = .35V
C51
.15V
5.4V
5.7V
EFFECT OF R42
adj. R47 (CHANGES
adj. R20 (CHANGES
FINAL SLOPE = 12µA/.1 + 2
EFFECT OF R47 + R44
11B-1
2.3V
1.V
INITIAL SLOPE = .2V MSEC = 20µA/.1µF
VERT SYNC INPUT
.2V
193 µSEC
16.6 MSEC

DWG. NO.	SH	REV
0114-0191	2	P

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			





URVATURE)

AMPLITUDE)

A = .38 V/MSEC

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: L .599 ± .003; 6K .999 ± .004; 1.000 1.499 ± .005

DRAWN: [illegible] DATE: 6-25-80

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV | DATE

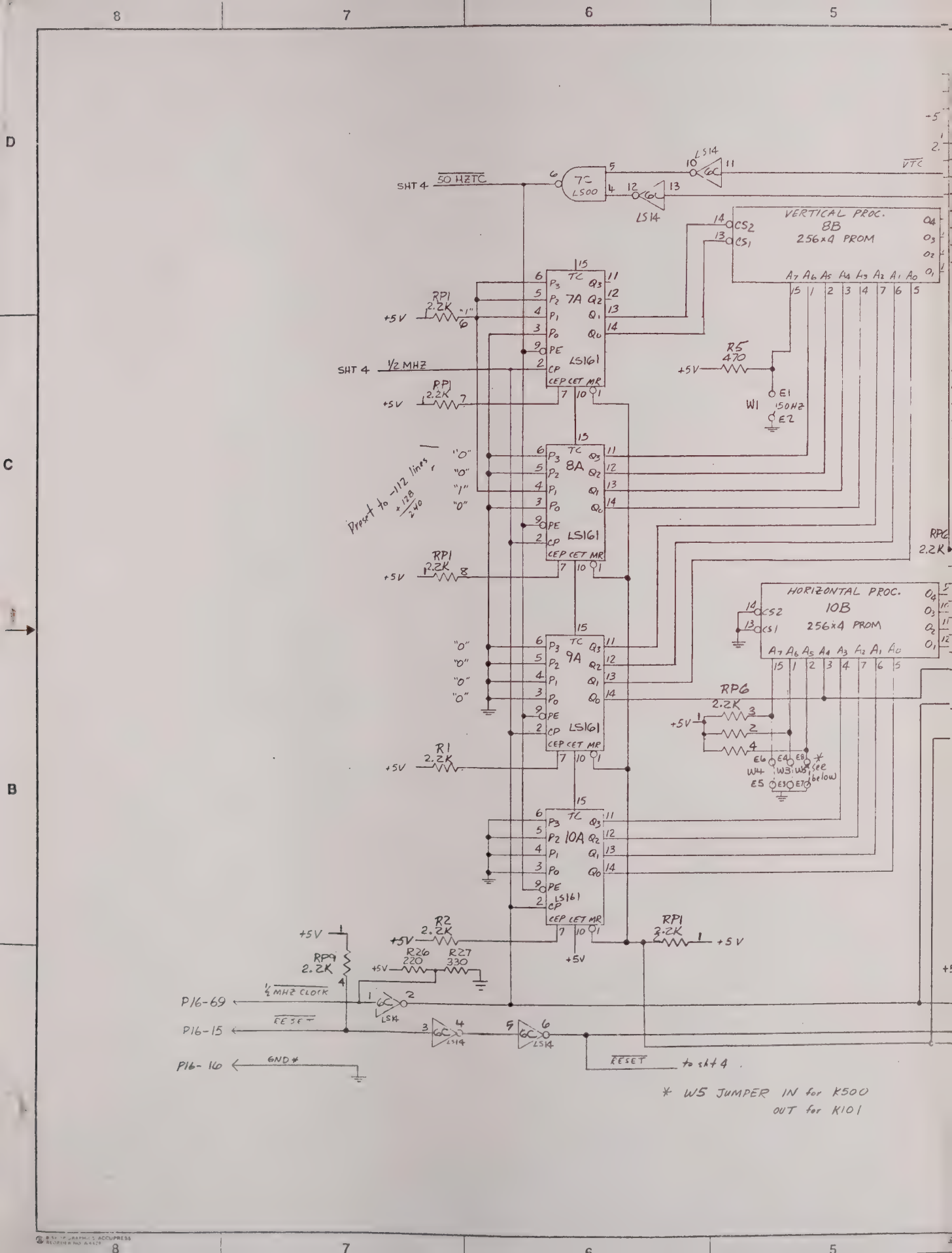
DASH NO | NUMBER | QTY | NEXT ASSEMBLY

GOULD biomation

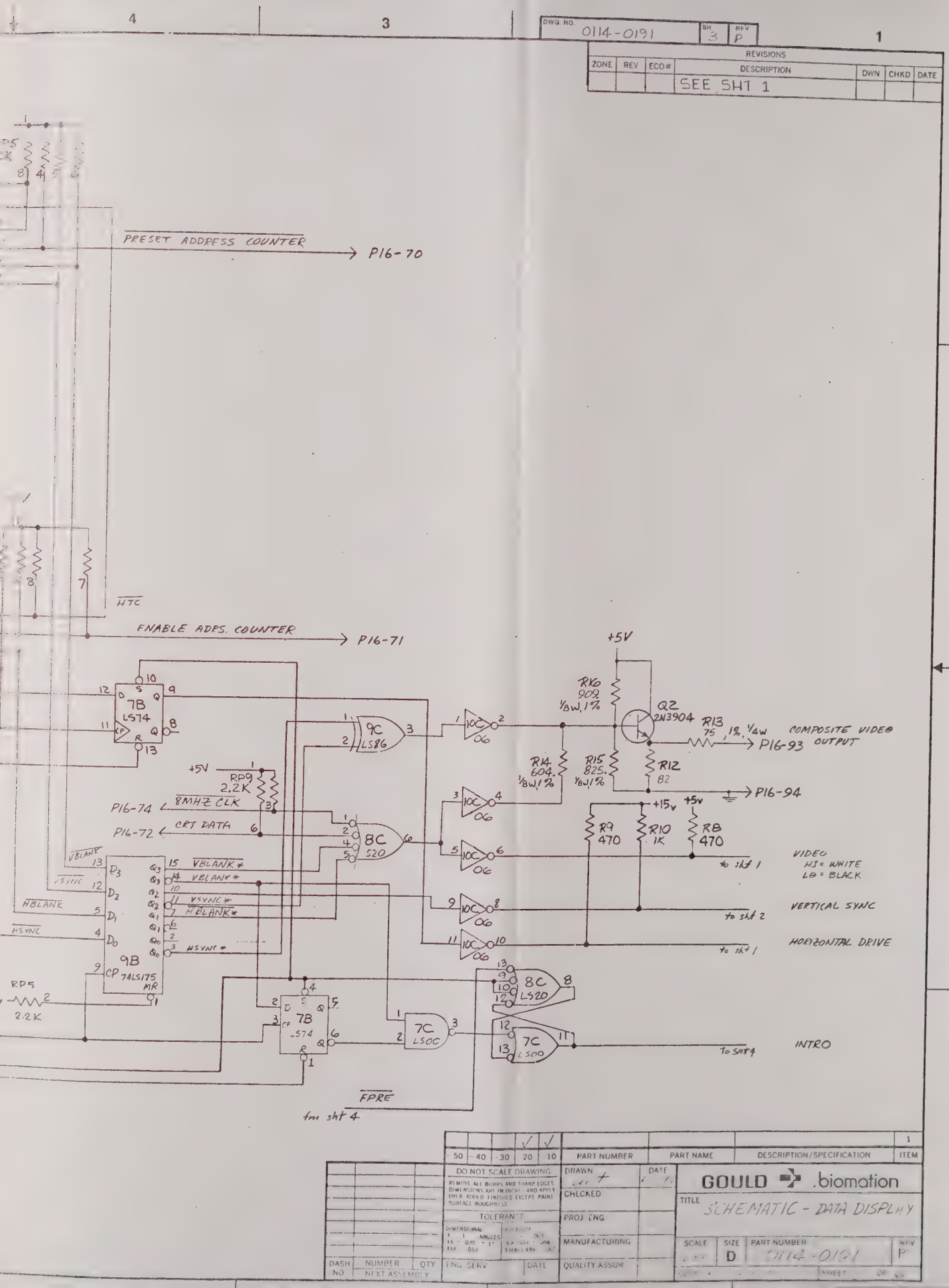
TITLE: SCHEMATIC DATA DISPLAY

SCALE | SIZE D | PART NUMBER 0114-0191 | REV P

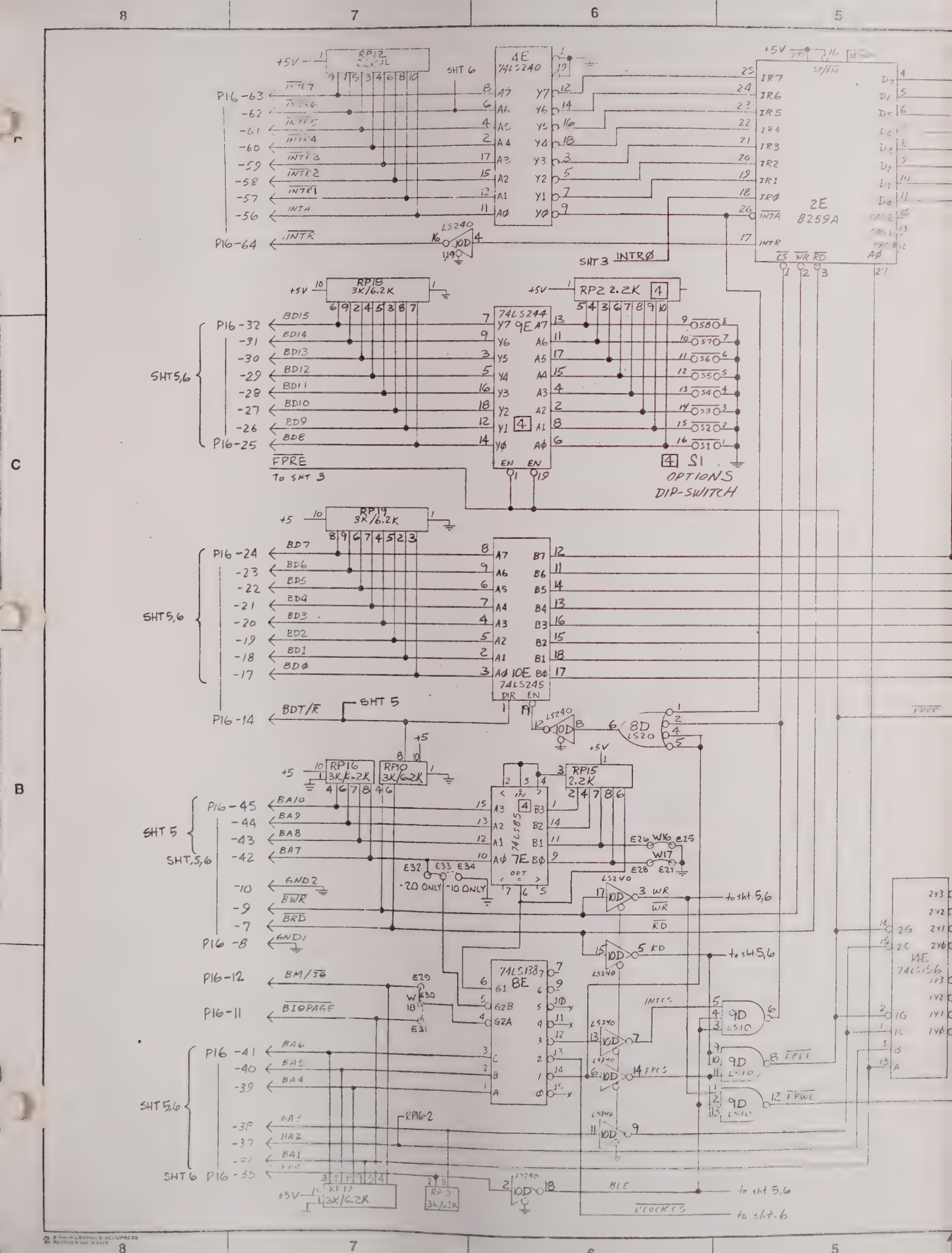
CODE | SHEET 2 OF 6



SHT 4
50 HZTC
7C
LS00
LS14
VTC
VERTICAL PROC.
8B
256x4 PROM
CS2
CS1
A7 A6 A5 A4 A3 A2 A1 A0
7A
LS161
RP1
2.2K
+5V
SHT 4
1/2 MHZ
R5
470
W1
E1
50HZ
E2
8A
Preset to -112 lines
+128
240
"0"
"1"
9A
HORIZONTAL PROC.
10B
256x4 PROM
RP6
2.2K
E6 E4 E8
W4 W3 W5
E5 E3 E7
* see below
R1
10A
R2
RP9
R26
220
R27
330
1/2 MHZ CLOCK
P16-69
RESET
P16-15
P16-16
GND *
to sht 4
* W5 JUMPER IN for K500
OUT for K101



DWG. NO. 0114-0191
SH 3
REV P
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SHT 1
PRESET ADDRESS COUNTER
P16-70
HTC
ENABLE ADRS. COUNTER
P16-71
7B LS74
9C LS86
10C 06
+5V
R16 909 1/8W, 1%
Q2 2N3904
R13 75, 1%, 1/4W
COMPOSITE VIDEO OUTPUT
P16-93
R14 604. 1/8W, 1%
R15 825. 1/8W, 1%
R12 82
P16-94
RP9 2.2K
P16-74
8MHZ CLK
P16-72
CRT DATA
8C S20
+15v
R9 470
R10 1K
R8 470
VIDEO
HI = WHITE
LO = BLACK
to sht 1
VERTICAL SYNC
to sht 2
HORIZONTAL DRIVE
to sht 1
VBLANK
VSYNC
HBLANK
HSYNC
9B 74LS175
VBLANK*
VSYNC*
HBLANK*
HSYNC*
RP5 2.2K
8C LS20
7C LS00
INTRO
to SHT 4
FPRE
fm sht 4
-50
-40
-30
20
10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY
OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS
TOLERANCE
DRAWN
DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC - DATA DISPLAY
SCALE
SIZE D
PART NUMBER 0114-0191
REV P
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
SHEET



RP12
4E
74LS240
SHT 6
P16-63
-62
-61
-60
-59
-58
-57
-56
P16-64
INTR
LS240
2E
8259A
SHT 3
INTRØ
RP18
3K/6.2K
RP2 2.2K
74LS244
9E
P16-32
-31
-30
-29
-28
-27
-26
P16-25
SHT5,6
FPRE
To SHT 3
S1
OPTIONS
DIP-SWITCH
RP19
3K/6.2K
P16-24
-23
-22
-21
-20
-19
-18
-17
P16-14
BDT/R
SHT 5
10E
74LS245
8D
LS20
RP16
3K/6.2K
RP10
3K/6.2K
RP15
2.2K
74LS85
7E
P16-45
-44
-43
-42
-10
-9
-7
P16-8
SHT 5
SHT,5,6
GND2
BWR
BRD
GND1
-20 ONLY
-10 ONLY
to sht.5,6
74LS138
8E
P16-12
P16-11
BM/IO
BIOPAGE
P16-41
-40
-39
-38
-37
-36
P16-35
SHT 6
RP16-2
RP17
3K/6.2K
RP3
3K/6.2K
BLE
CLOCKCS
to sht 5,6
to sht.6
14E
74LS156
9D
LS10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			

SHT 3 — 1/2 MHZ

SHT 3 — 50 HZTC

17E LS74

R54 2.2K +5v

R60 2.2K +5v

BEEPER

R56 VOLUME 1K

R57 39Ω, 1/2W +15V

R55 2.2K +5v

16E 74LS161

15E 74LS161

R53 2.2K +5v

RESET

from sht. 3

-20 ONLY

13E 74LS244

74LS273 12E

RP20 2.2K

KEYBOARD INTERFACE

P15-8 -7 -6 -5 -4 -3 -2 P15-1

P15-16 -15 -14 -13 -12 -11 -10 -9

LED OUTPUTS

LØ = LIGHTED

HI = OFF

P15 -24 -23 -22 -21 -20 -19 -18 -17

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± 0.10 ± 1°; XXX ± 010

NOTE SIZE: 0 to 999 ± 003; 600 to 999 ± 004; 1000 to 1499 ± 005

DASH NO	NUMBER NEXT ASSEMBLY	QTY

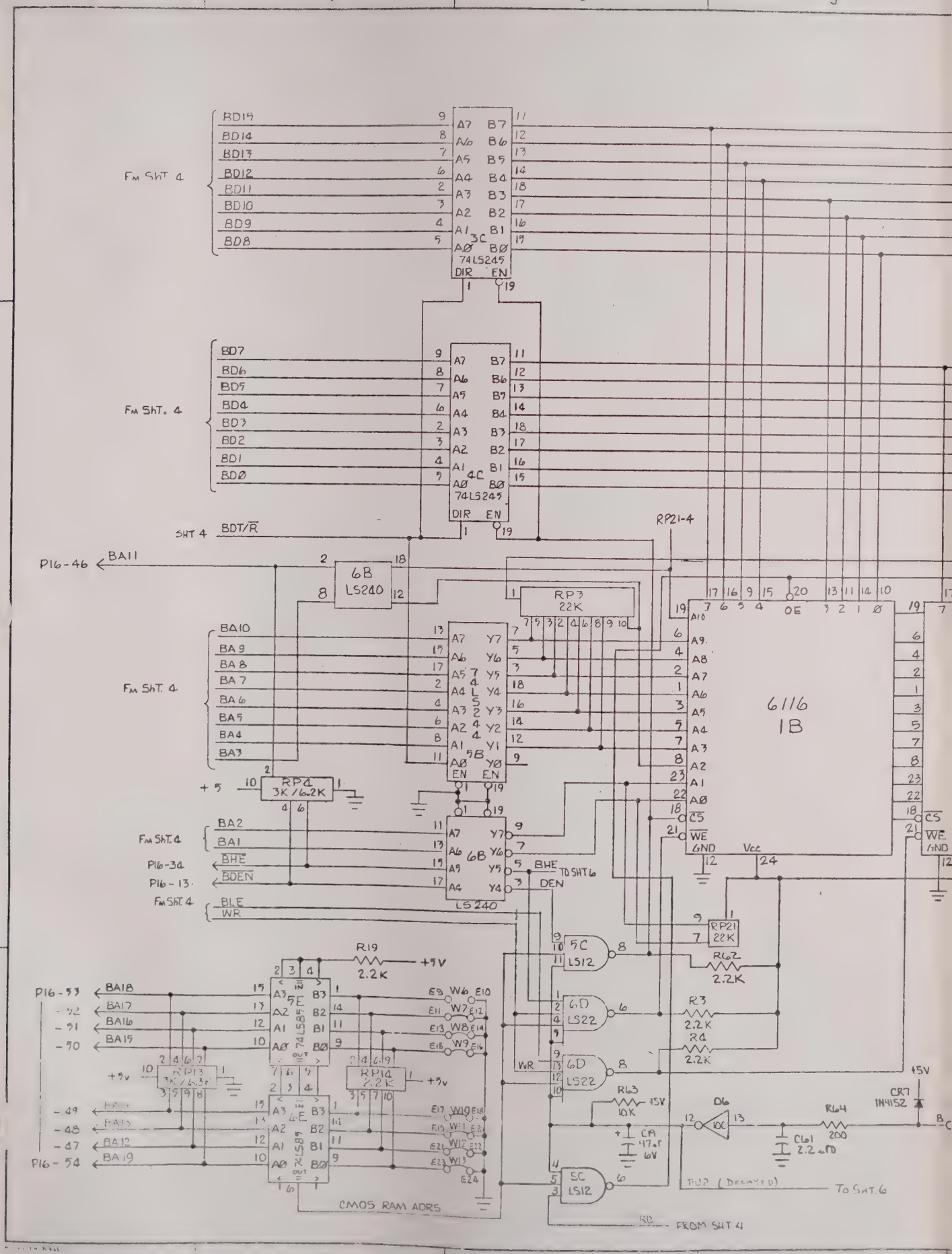
DRAWN	DATE
CHECKED	
PROJ ENG	
MANUFACTURING	
QUALITY ASSUR	
LNG SERV	DATE

GOULD biomation

TITLE SCHEMATIC
DATA DISPLAY

SCALE	SIZE	PART NUMBER	REV
	D	0114-0191	P

CODE | SHEET 4 OF 20



8
7
6
5
FM SHT 4
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
3C
74LS245
DIR
EN
FM SHT. 4
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
4C
74LS245
SHT 4
BDT/R
P16-46
BA11
6B
LS240
RP21-4
RP3
22K
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
74LS244
5B
6116
1B
OE
CS
WE
GND
Vcc
+5
RP4
3K/6.2K
BA2
BA1
P16-34
BHE
P16-13
BDEN
BLE
WR
6B
LS240
BHE
TO SHT 6
DEN
RP21
22K
R62
2.2K
5C
LS12
6D
LS22
R3
2.2K
R4
2.2K
R19
2.2K
+5V
P16-53
BA18
BA17
BA16
BA15
5E
74LS85
RP13
3K/6.3K
RP14
2.2K
6E
74LS85
R63
10K
CA
47.0
6V
D6
10C
R64
200
C61
2.2
CR7
1N4152
P16-54
BA12
BA19
CMOS RAM ADRS
PUP (DELAYED)
TO SHT. 6
RD
FROM SHT 4

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			

RP7 22K

RP8 22K

THIS SHEET -20 ONLY

R65 2.2K

6116 3B

VBATT → TO SHT 6
15 MA MAX OPERATING

R66 390.

Q1 2N3906

+5V

C5 0.1 100V

C6 0.1 100V

R61 51

E36

E35

+2.4V BAT B1

R58 2.2K

R7 270

2N3904 Q6

R50 3.3K

R51 680.

C57 .01μf +15V

AGND

P15-30 ← V BATT

11E LF356

P15-39 ← -15V

-40 ←

C55 33μf +25V

C56 .01μf

AGND

LS14

P0P → P116-79

PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY EVEN AFTER FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DRAWN Leaf DATE 12-11-80

CHECKED

PROJ ENG

MANUFACTURING

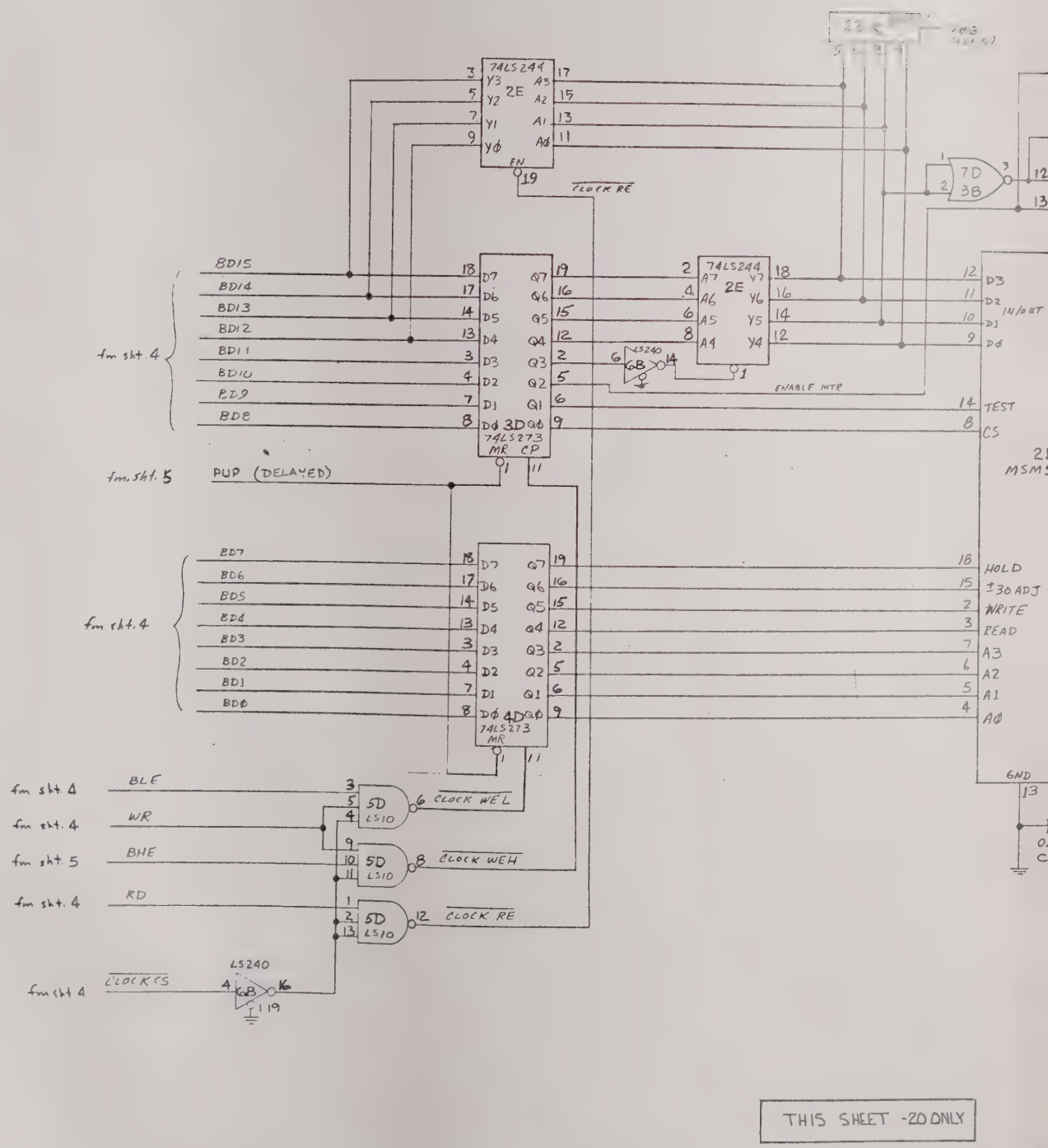
QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC DATA DISPLAY

SCALE — SIZE D PART NUMBER 0114-0191 REV P

CODE SHEET 5 OF 6

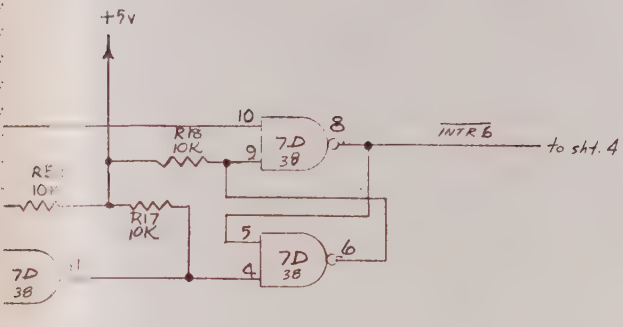


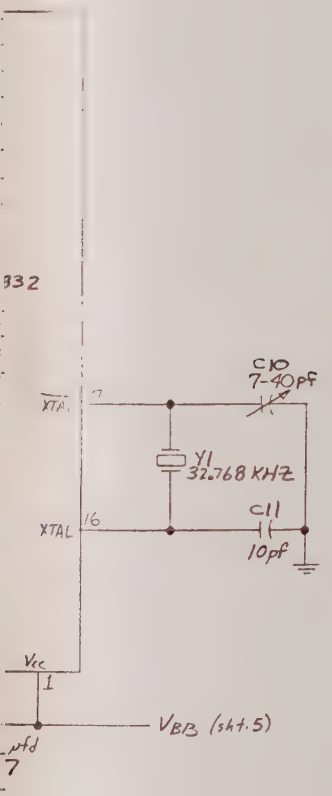
THIS SHEET -2D ONLY

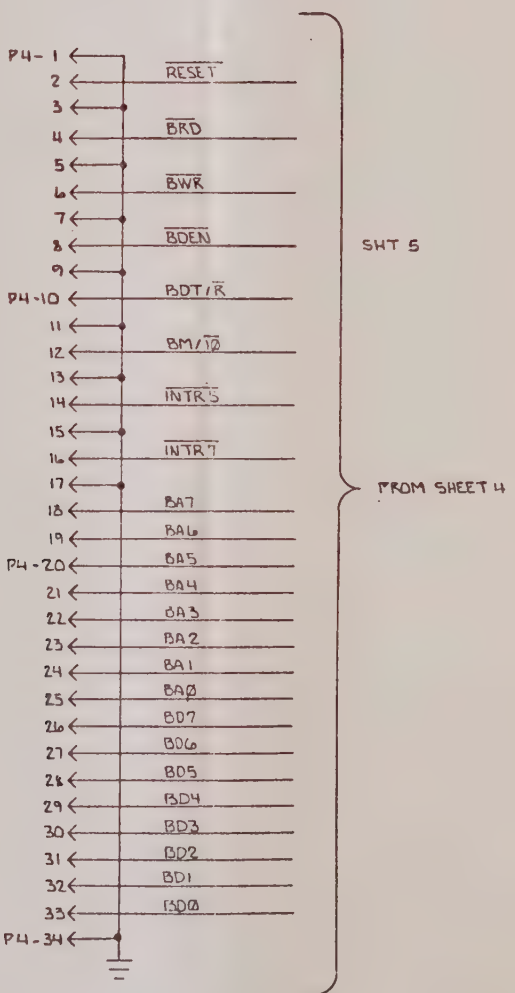
DWG NO 0114-0171 | SH 6 | REV P

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DA
			SEE SHT 1			







PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

50 | 40 | 30 | 20 | √ 10

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONS

ANGLES

DRAWN | DATE

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

GOULD biomation

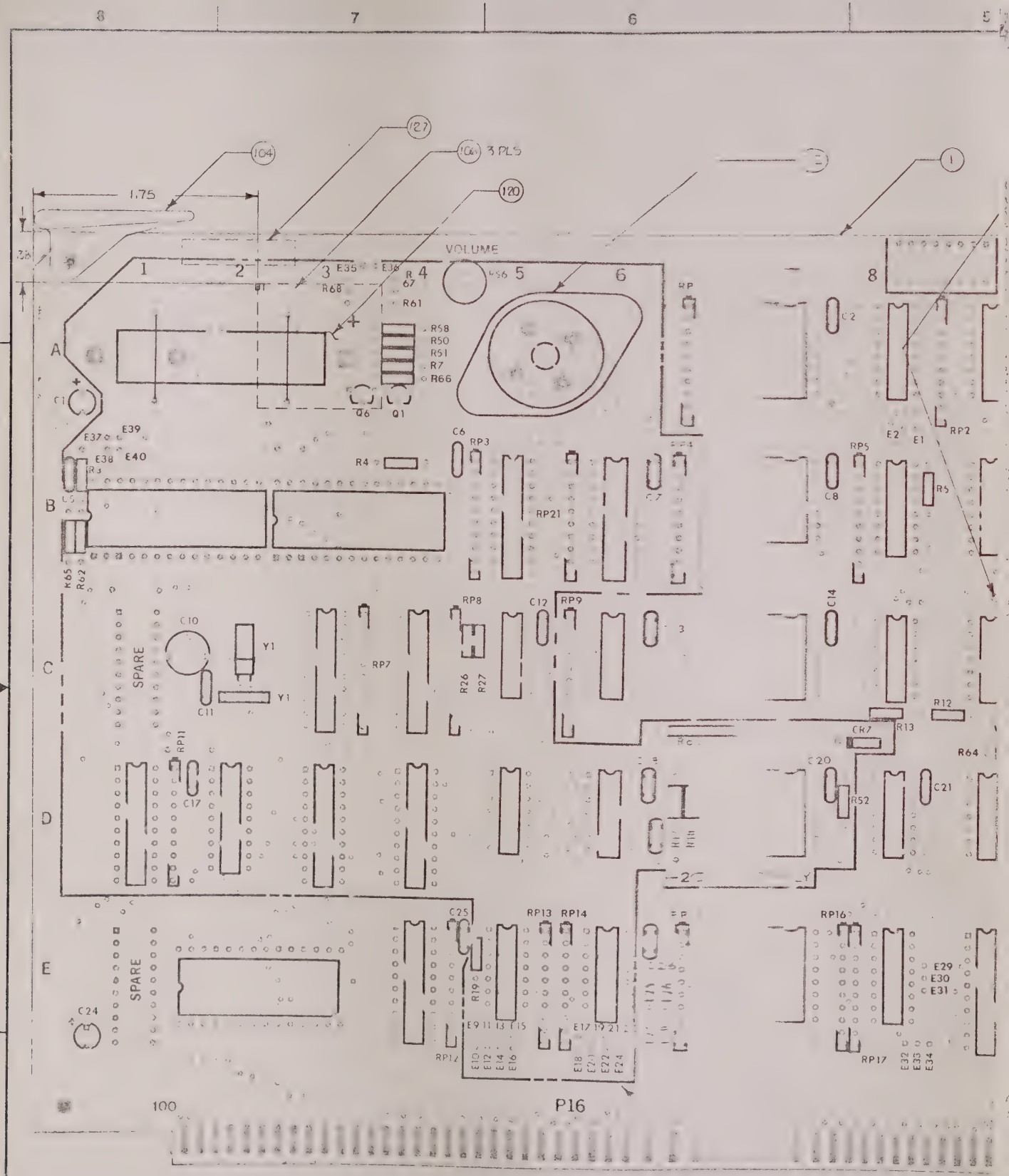
TITLE SCHEMATIC - DATA DISPLAY

SCALE | SIZE D | PART NUMBER 0114-0191 | REV P

CODE | SHEET 6 OF 6

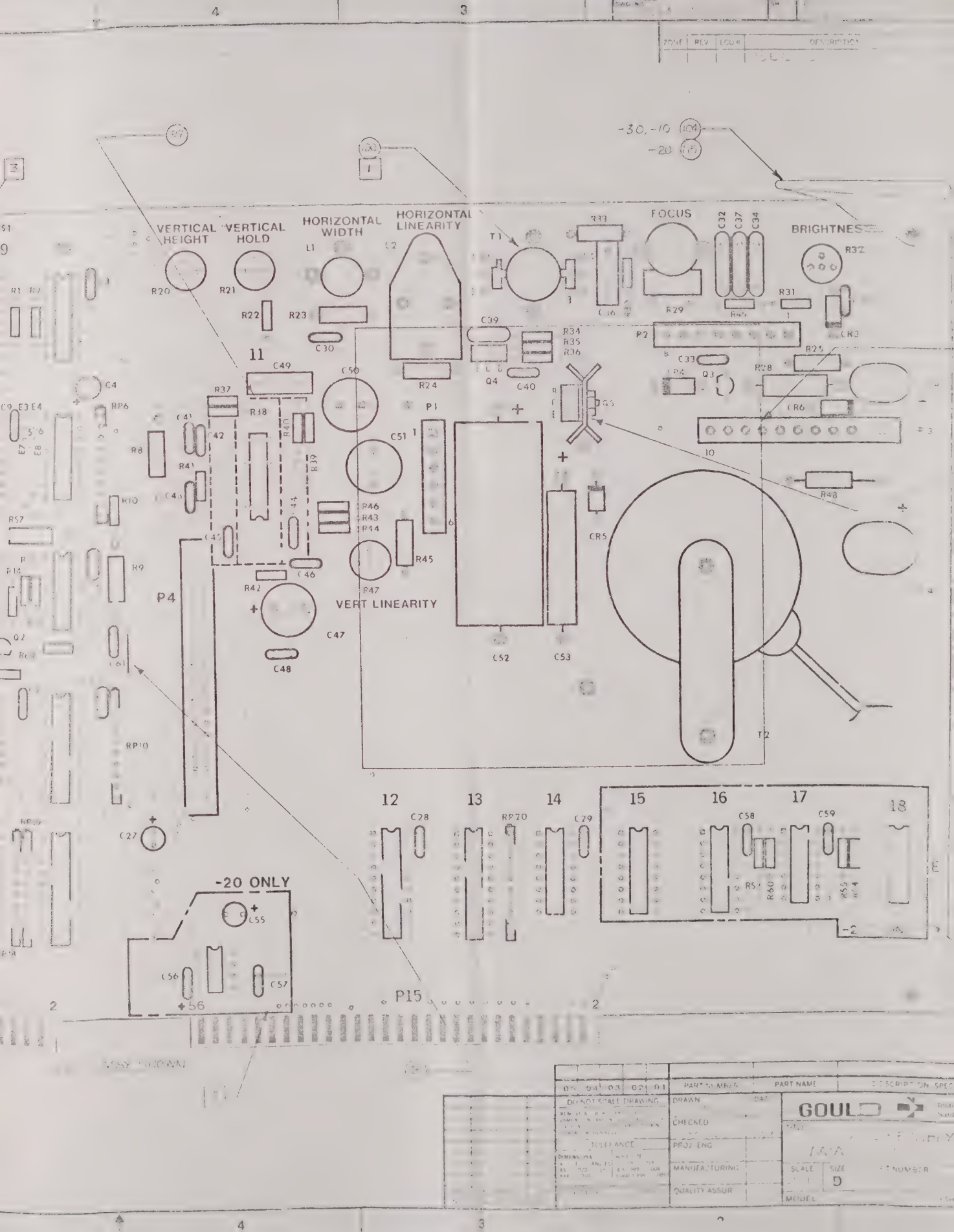
DASH NO | NUMBER | QTY | NEXT ASSEMBLY

ENG SERV | DATE



NOTES:

1. REMOVE MOUNTING HARWARE SUPPLIED WITH T1, USE ITEM (10) TO SECURE TO BOARD
2. IC'S 7E, 9E, R42 & S1 ARE -10 ONLY
3. COMPONENTS IN THIS AREA PLUS R57 ARE -20 ONLY EXCEPT FOR R26 & R27.



VERTICAL HEIGHT
VERTICAL HOLD
HORIZONTAL WIDTH
HORIZONTAL LINEARITY
FOCUS
BRIGHTNESS
VERT LINEARITY
-20 ONLY
-30, -10
-20
P1
P2
P4
P15
T1
T2
11
12
13
14
15
16
17
18
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
PART NUMBER
PART NAME
DESCRIPTION SPEC
GOULD
SCALE
SIZE
D
MODEL

JUMPER	AS ETCHED	-20 K101/K102	-10/-30 K500/K105	DESCRIPTION
E1 TO E2	OUT		JUMPER FOR 50HZ ONLY	CRT SCAN RATE IN=50HZ OUT=60HZ
E3 TO E4	OUT			NOT USED
E5 TO E6	OUT			NOT USED
E7 TO E8	OUT		JUMPER	IN = K500 HORIZ. SCAN OUT=K101
E9 TO E10	OUT			A18
E11 TO E12	IN			A17
E13 TO E14	IN			A16
E15 TO E16	IN			A15 } K101 CMOS RAM
E17 TO E18	IN			A14 } ADDRESS SELECTION
E19 TO E20	IN			A13
E21 TO E22	IN			A12
E23 TO E24	IN			A19
E25 TO E26	IN			A8 } K500 MEM MAPPED I/O
E27 TO E28	IN			A7 } ADDRESS DECODE
E29 TO E30	IN		CUT	IN SELECTS I/O MAPPED I/O (K101)
E30 TO E31	OUT		JUMPER	IN SELECTS MEM MAPPED I/O (K500)
E32 TO E33	IN		CUT	IN FOR K101
E33 TO E34	OUT		JUMPER	IN FOR K500

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A					
	B		PRODUCTION RELEASE PER FRN 3[illegible]			
	C	[illegible]A	REV'D PER ECO	[illegible]	[illegible]	[illegible]

ECO PENDING # 3865P 3906P

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DATE

DRAWN

CHECKED

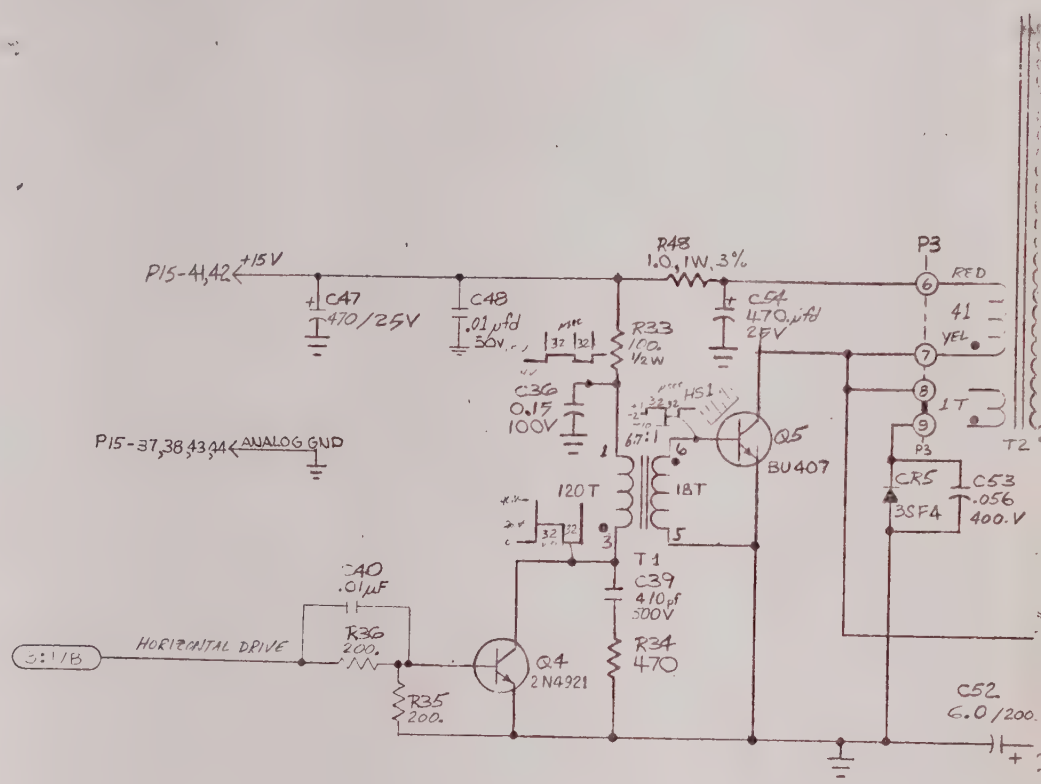
PROJ ENG.

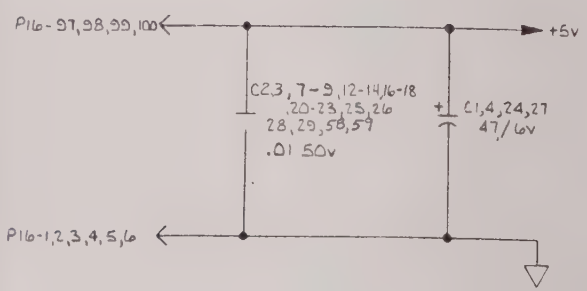
GOULD biomation

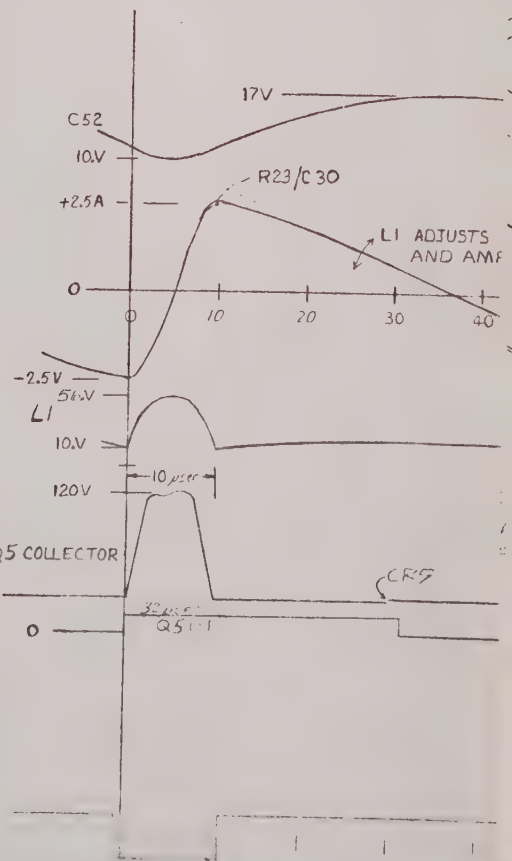
TITLE ASSEMBLY [illegible] DISPLAY BD

SCALE | SIZE D | PART NUMBER [illegible] | REV C

SHEET 1 OF

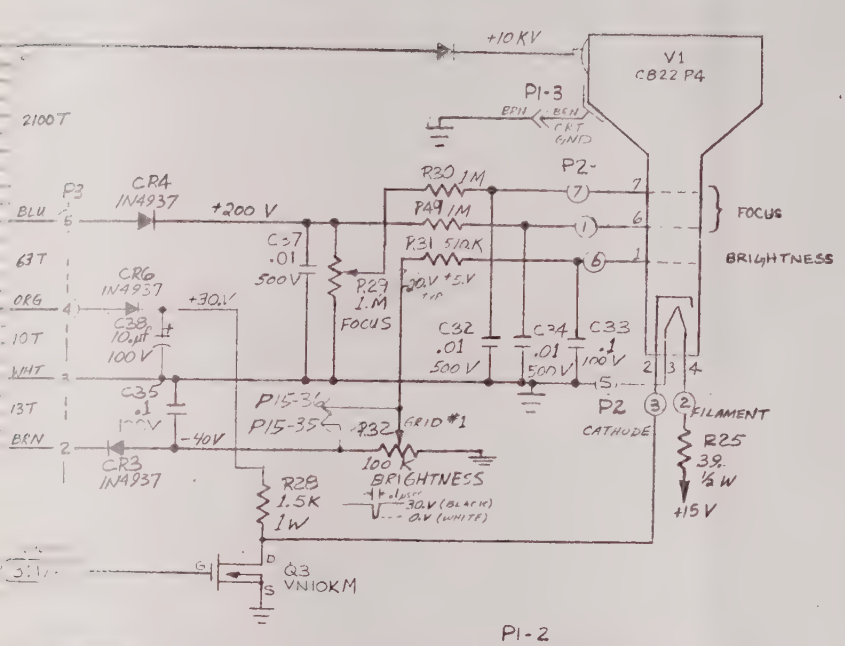


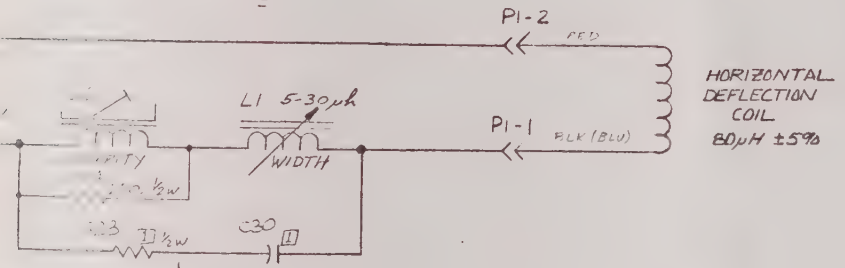


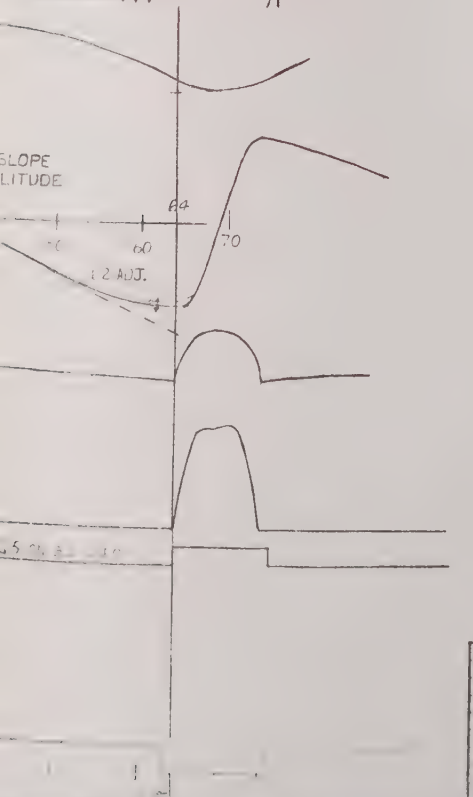


NOTES

1. SELECTED AT TEST. NOT NORMALLY USED. R23 = 100 Ω 30 = .002 µF MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ LINEARITY AT LEFT SIDE OF DISPLAY
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. -10 ONLY







ECO PENDING # 3863P
3906P

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

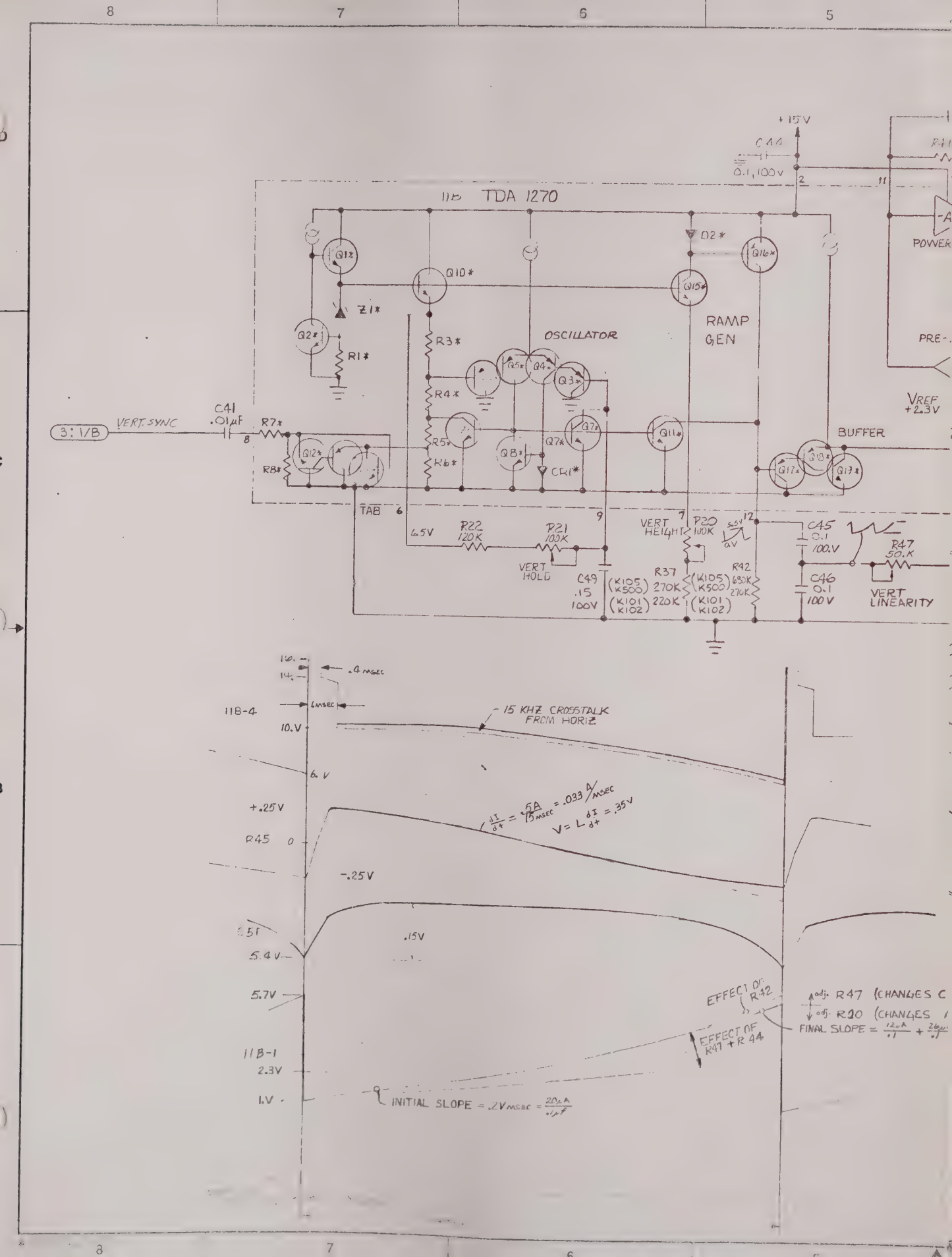
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING

GOULD biomation

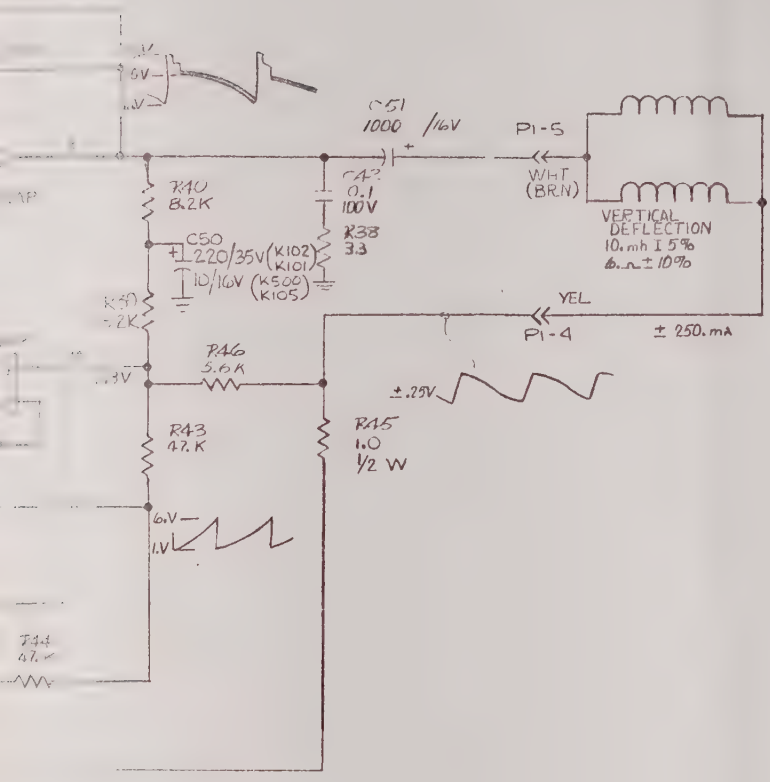
SCHEMATIC
TA DISPLAY PWB

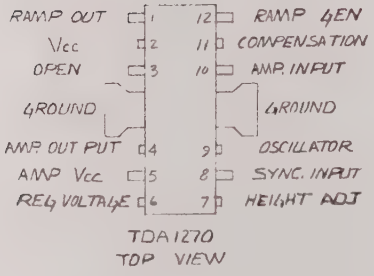
SIZE D | PART NUMBER 2011

SHEET



8
7
6
5
+15V
C44
0.1, 100V
11B TDA 1270
D2*
Q1*
Q10*
Q16*
Q15*
Z1*
Q2*
R1*
R3*
OSCILLATOR
RAMP GEN
Q5*
Q4*
Q3*
R4*
R5*
R6*
Q7*
Q8*
Q11*
CR1*
Q12*
R8*
3:1/B
VERT. SYNC
C41
.01μF
R7*
TAB
6.5V
R22
120K
R21
100K
VERT HOLD
C49
.15
100V
VERT HEIGHT
P20
100K
R37
270K
220K
R42
680K
270K
C45
0.1
100V
C46
0.1
100V
R47
50.K
VERT LINEARITY
BUFFER
Q17*
Q18*
Q13*
POWER
PRE-
VREF
+2.3V
11B-4
.4 MSEC
1 MSEC
10.V
6.V
15 KHZ CROSSTALK FROM HORIZ
+.25V
R45
0
-.25V
.15V
5.4V
5.7V
11B-1
2.3V
1.V
INITIAL SLOPE = .2V MSEC = 20μA / .1μF
EFFECT OF R42
EFFECT OF R47 + R44
adj. R47 (CHANGES C
adj. R20 (CHANGES
FINAL SLOPE = 12μA / .1 + 26μ / .1





TDA1270
TOP VIEW

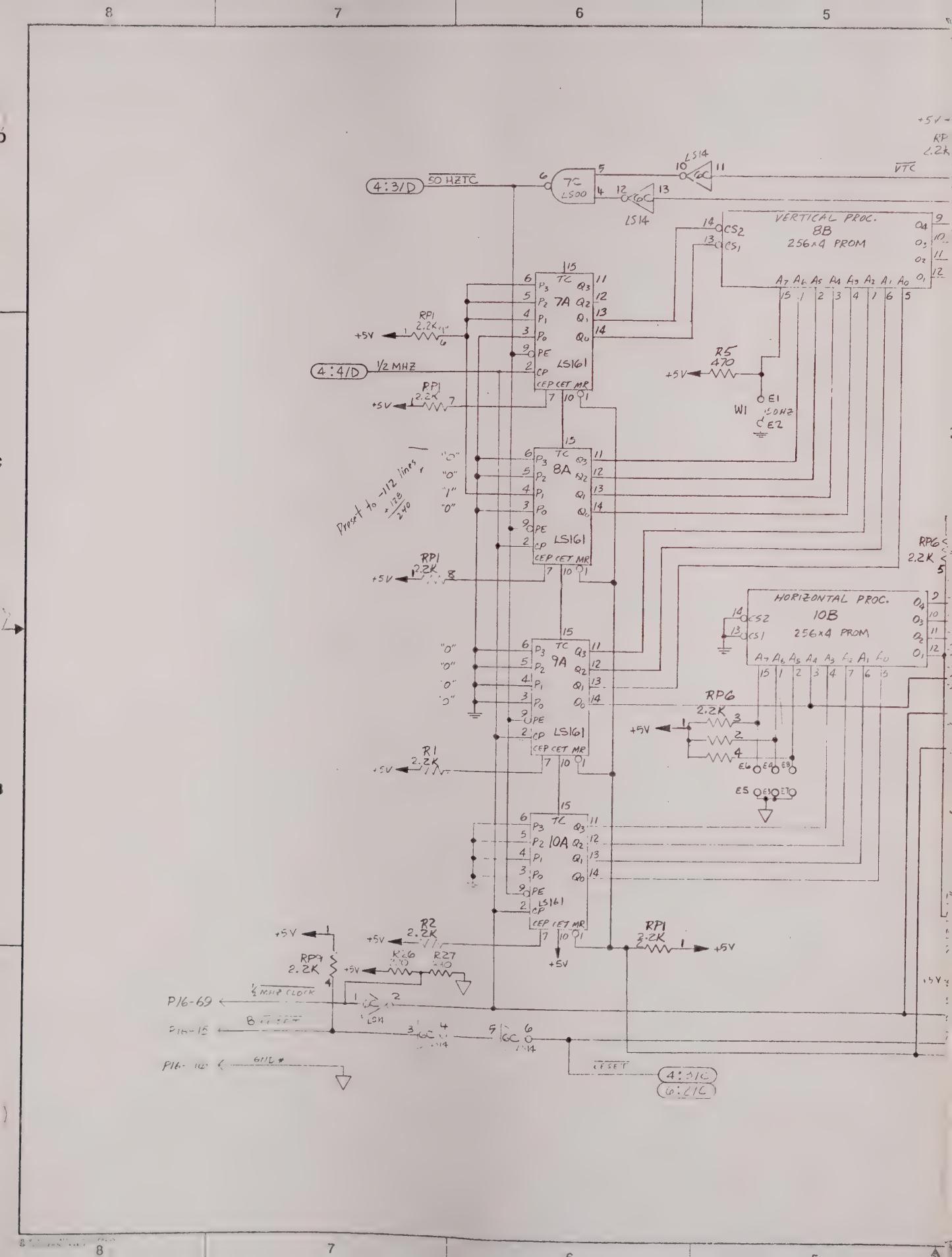
URVATURE)
MPLITUDE)
= .38 V/msec

50 40 30 20 10 PART NUMBER PART NAME DESCRIPTION SPECIFICATION ITEM

GOULD biomation

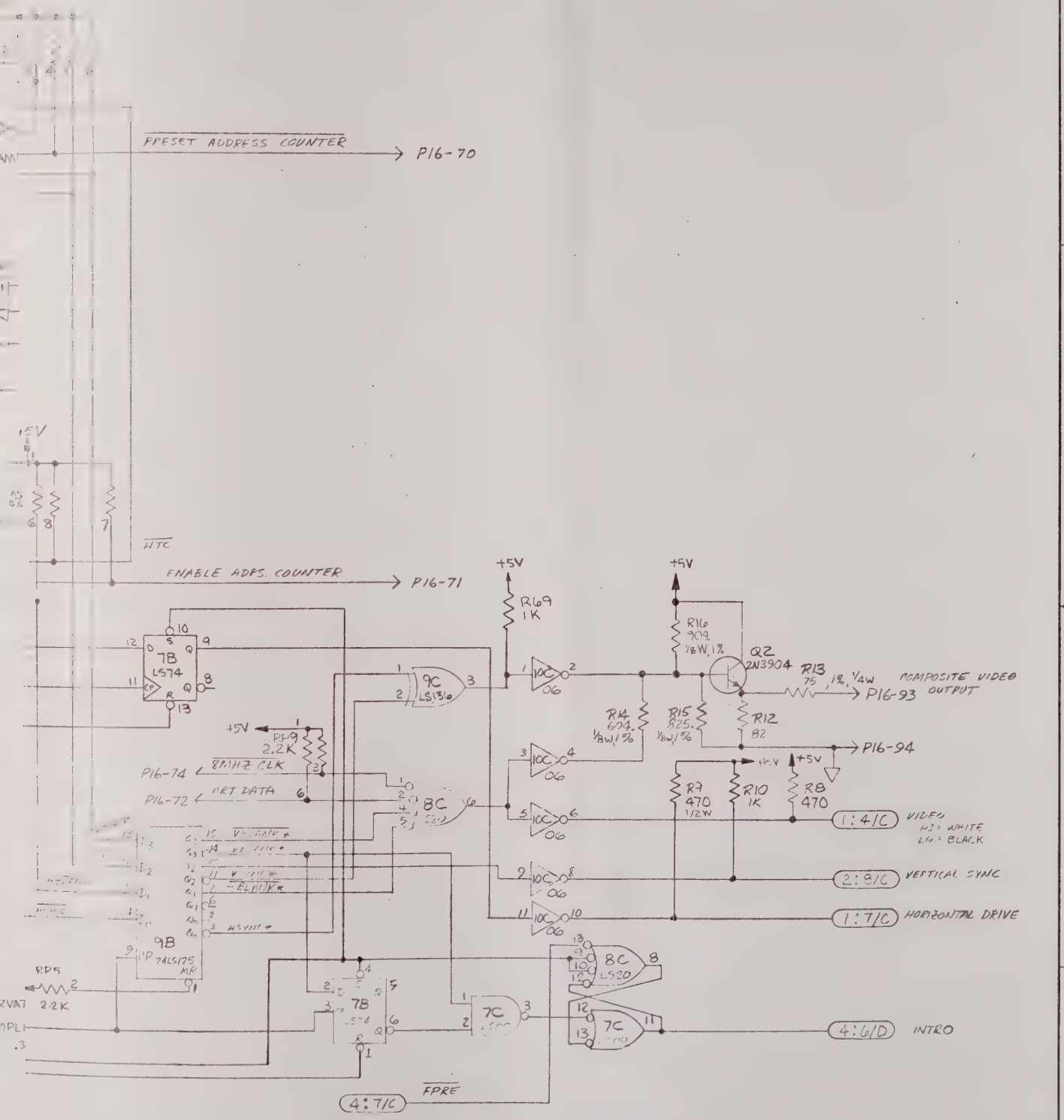
SCHEMATIC

D



8
7
6
5
4:3/D
50 HZTC
7C
LS00
LS14
VTC
VERTICAL PROC.
8B
256x4 PROM
CS2
CS1
7A
LS161
RP1
2.2K
+5V
4:4/D
1/2 MHZ
R5
470
W1
E1
E2
8A
Preset to -112 lines
+128
240
9A
HORIZONTAL PROC.
10B
256x4 PROM
RP6
2.2K
R1
10A
R2
RP9
R26
R27
P16-69
P16-15
P16-16
GND *
4:3/C
6:2/C

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



50	40	30	✓ 20	✓ 10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

DRAWN	DATE
CHECKED	
PROJ. ENG	
MANUFACTURING	
QUALITY ASSUR	

GOULD biomation

TITLE

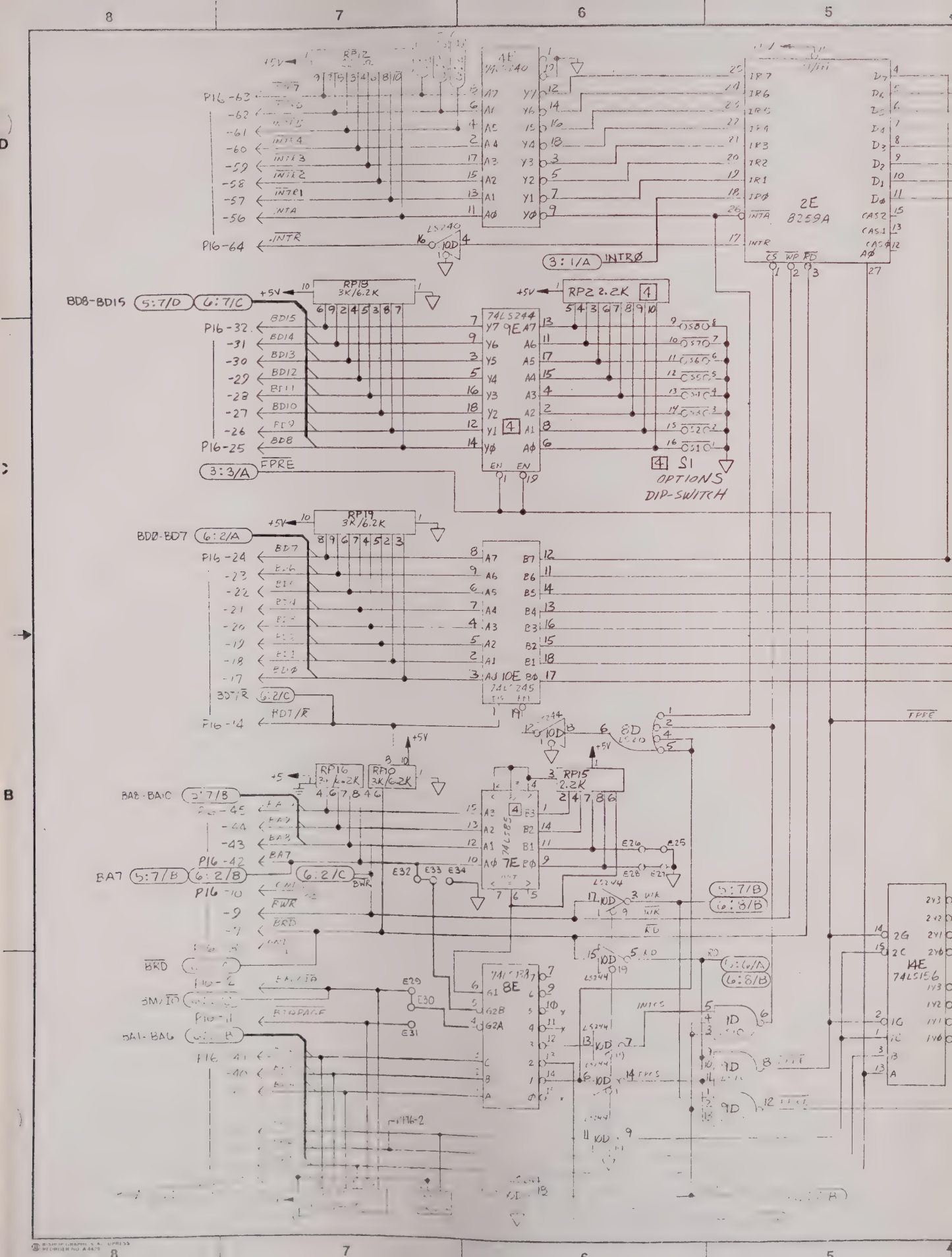
WB

SCALE	SIZE	PART NUMBER	REV
	D	0114-2011	C

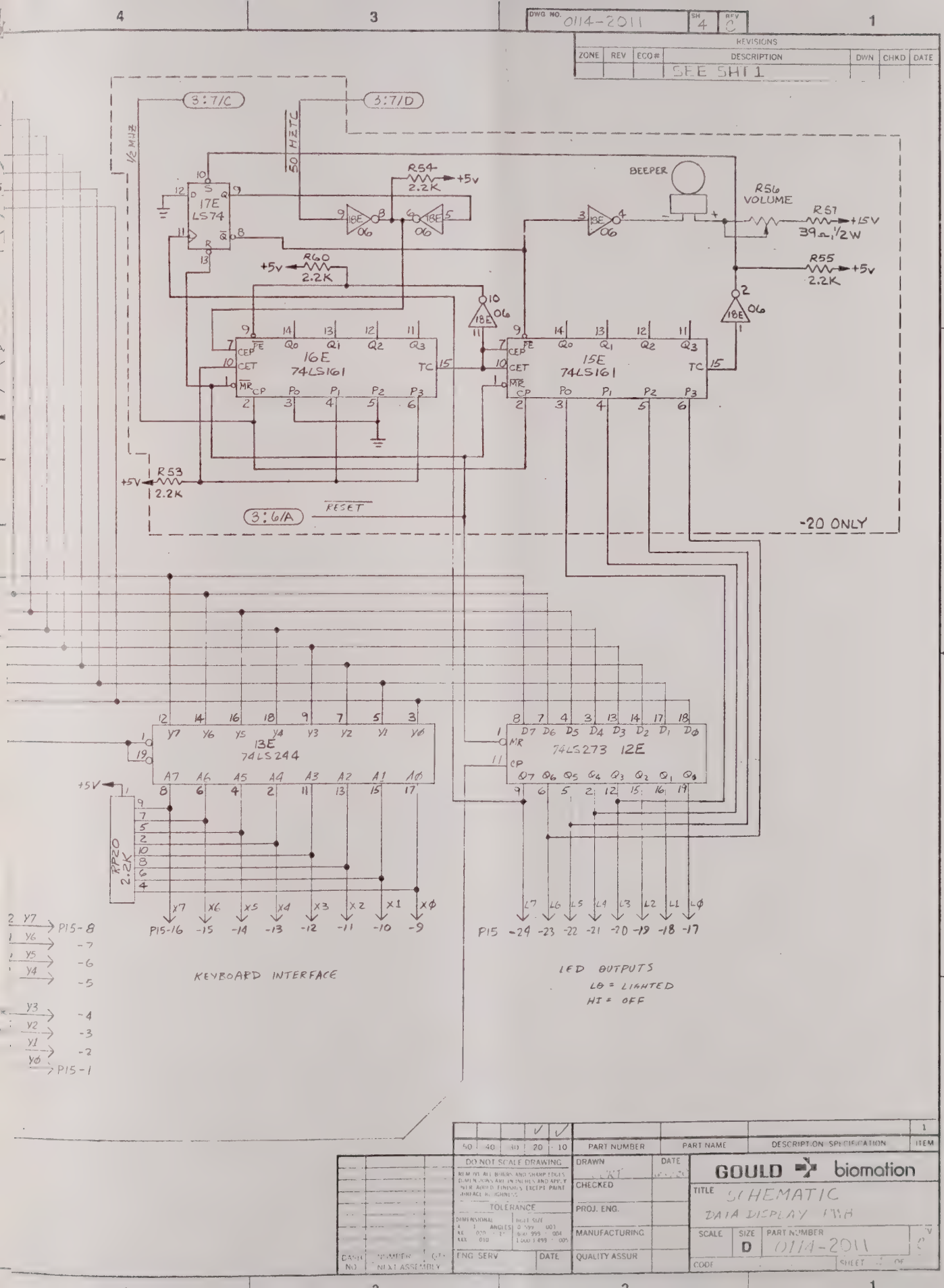
CODE SHEET OF

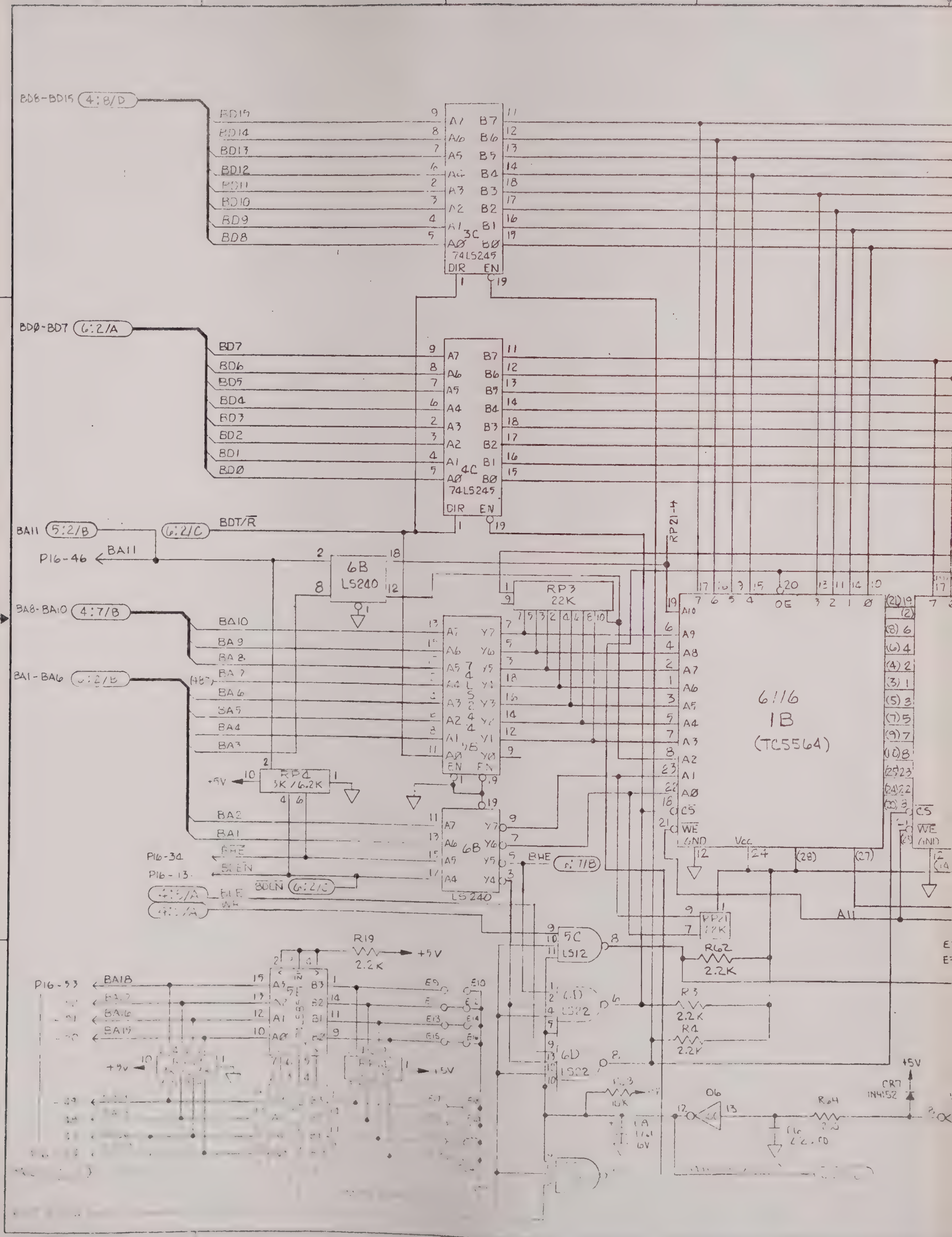
ITEM	NUMBER	QTY
	NEXT ASSEMBLY	

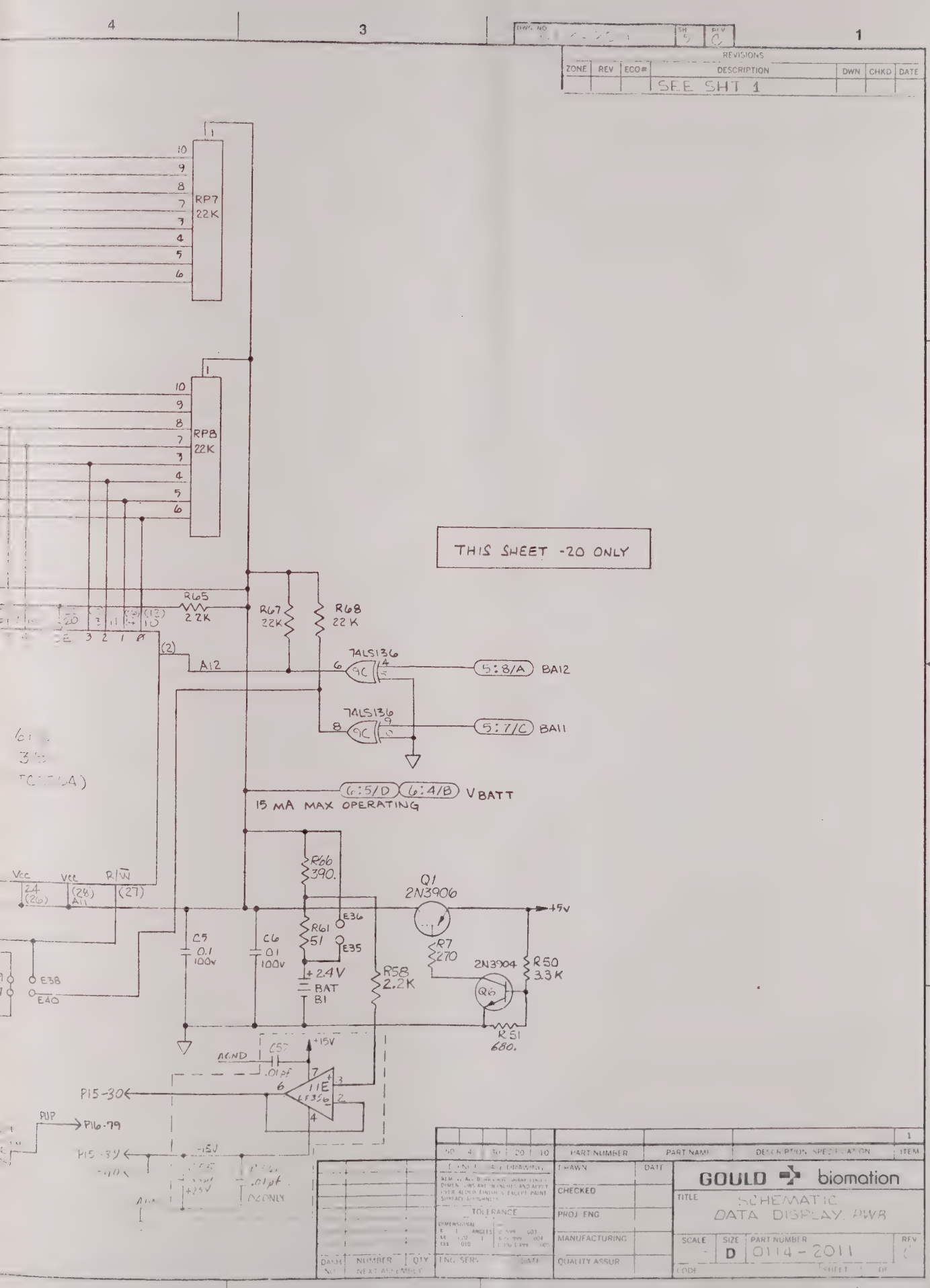
LNG SERV DATE



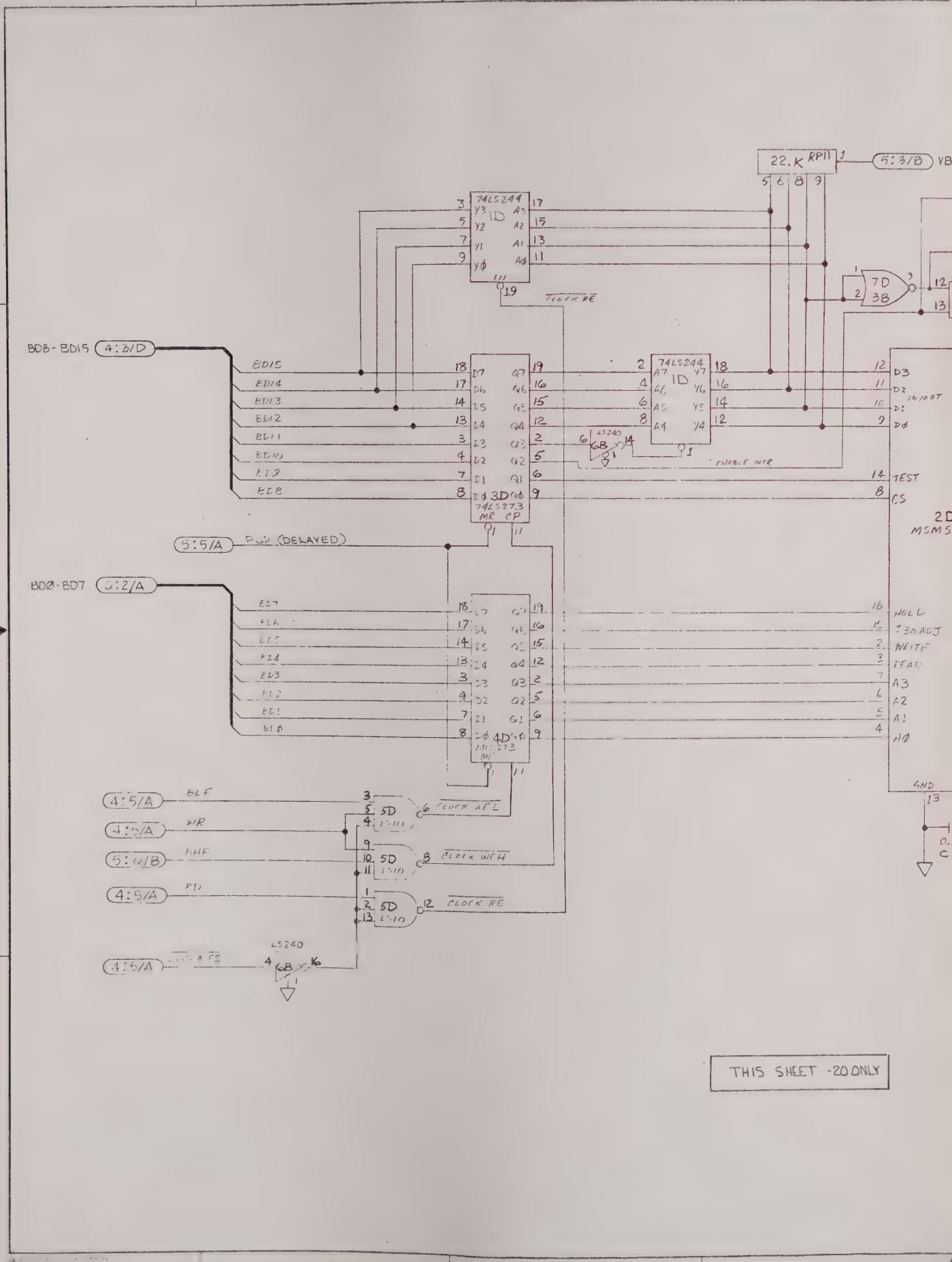
8
7
6
5
D
C
B
RP12
4E
74LS240
2E
8259A
3:1/A
INTRØ
RP18
3K/6.2K
RP2 2.2K
BD8-BD15
5:7/D
6:7/C
74LS244
9E
S1
OPTIONS
DIP-SWITCH
3:3/A
FPRE
RP19
3K/6.2K
BDØ-BD7
6:2/A
10E
74LS245
6:2/C
8D
RP16
RP10
3K/6.2K
RP15
2.2K
BA8-BA10
5:7/B
BA7
6:2/B
6:2/C
7E
74LS85
5:7/B
6:8/B
8E
74LS138
6:6/A
6:8/B
14E
74LS156
BA1-BA6


DWG NO. 0114-2011
SH 4
REV C
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
3:7/C
3:7/D
1/2 MHZ
50 HZ TC
17E LS74
R54 2.2K +5v
R60 2.2K +5v
BEEPER
R56 VOLUME
R57 39Ω 1/2W +15V
R55 2.2K +5v
16E 74LS161
15E 74LS161
R53 2.2K +5v
3:6/A
RESET
-20 ONLY
13E 74LS244
74LS273 12E
RP20 2.2K
P15-16 -15 -14 -13 -12 -11 -10 -9
P15 -29 -23 -22 -21 -20 -19 -18 -17
KEYBOARD INTERFACE
LED OUTPUTS
LØ = LIGHTED
HI = OFF
Y7 -> P15-8
Y6 -> -7
Y5 -> -6
Y4 -> -5
Y3 -> -4
Y2 -> -3
Y1 -> -2
Y0 -> P15-1
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DO NOT SCALE DRAWING
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
GOULD biomation
TITLE SCHEMATIC
DATA DISPLAY PWA
SCALE
SIZE D
PART NUMBER 0114-2011
CODE
SHEET

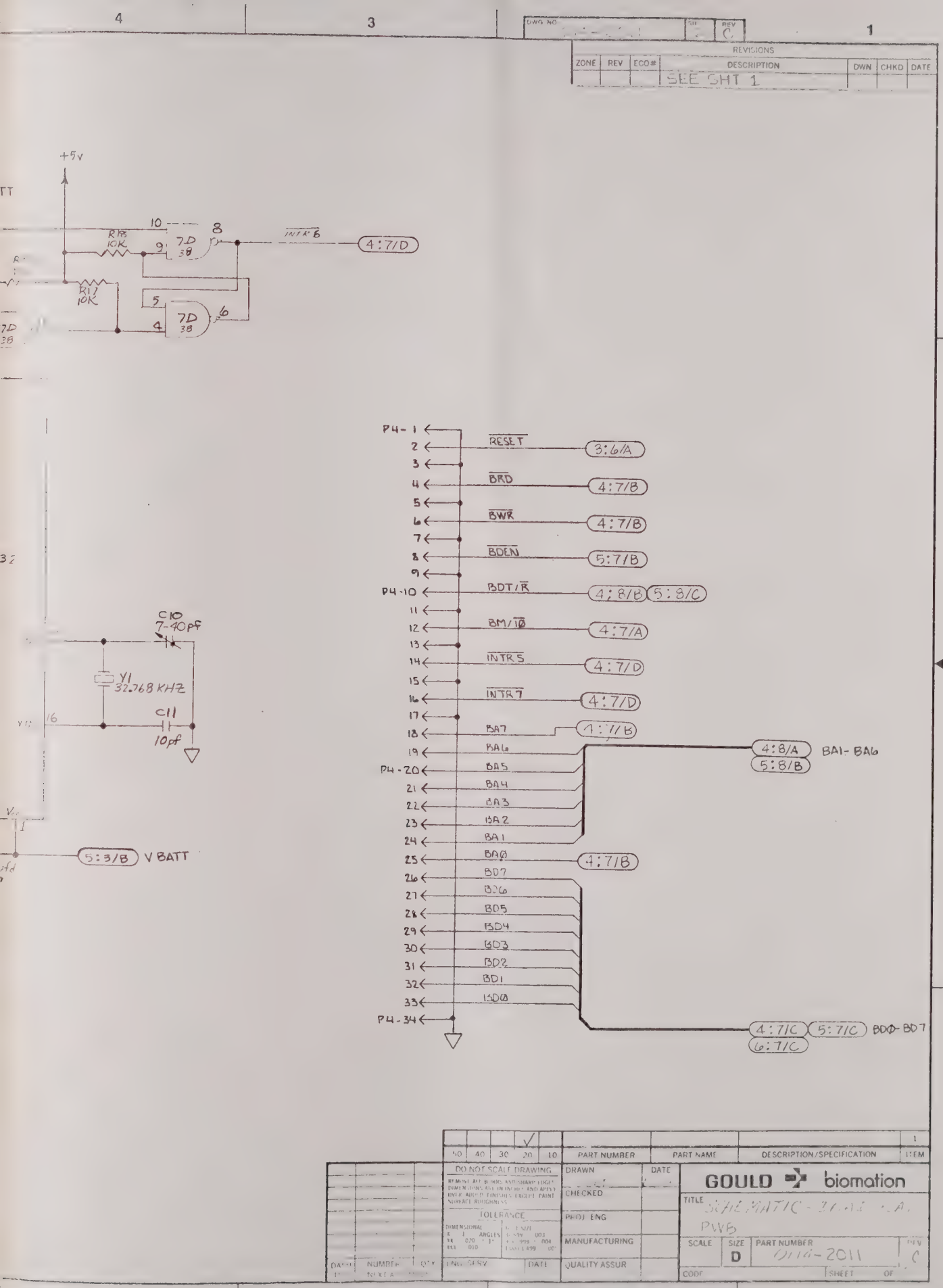

BD8-BD15 (4:8/D)
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
3C
74LS245
DIR
EN
BDØ-BD7 (6:2/A)
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BDØ
4C
74LS245
BA11 (5:2/B)
(6:2/C)
BDT/R
P16-46
BA11
6B
LS240
RP21-4
RP3
22K
BA8-BA10 (4:7/B)
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA1-BA6
RP4
3K/6.2K
+5V
BA2
BA1
6B
LS240
P16-34
P16-13
BHE
BDEN (6:2/C)
BLE
WR
6116
1B
(TC5564)
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
AØ
CS
WE
GND
Vcc
OE
RP21
22K
R62
2.2K
A11
5C
LS12
R19
2.2K
+5V
P16-33
BA18
BA17
BA16
BA15
E9
E10
E13
E14
E15
E16
R3
2.2K
R4
2.2K
6D
LS22
R63
10K
O6
R64
CR7
IN4152
+5V



REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SHT 1
RP7 22K
RP8 22K
THIS SHEET -20 ONLY
R65 22K
R67 22K
R68 22K
74LS136
5:8/A BA12
5:7/C BA11
A12
6:5/D 6:4/B VBATT
15 MA MAX OPERATING
R66 390.
Q1 2N3906
+5V
R61 51
E36
E35
C5 0.1 100v
C6 .01 100v
+2.4V BAT B1
R58 2.2K
R7 270
2N3904
R50 3.3K
Q6
R51 680.
E38
E40
Vcc
R/W
AGND
C57 .01pf
+15V
11E LF356
P15-30
P16-79
PUP
-15V
+25V
.01pf
.02 ONLY
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
TOLERANCE
DIMENSIONAL
ANGLES
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
GOULD biomation
TITLE
SCHEMATIC
DATA DISPLAY PWB
SCALE
SIZE
D
PART NUMBER
0114-2011
REV
CODE
SHEET
OF



22.K RP11
5:3/B
74LS244
1D
CLOCK RE
7D
38
BD8-BD15
4:3/D
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
3D
74LS273
MR CP
LS240
6B
ENABLE INTR
D3
D2
D1
D0
IN/OUT
TEST
CS
2D
MSM5
5:5/A
PUR (DELAYED)
BD0-BD7
6:2/A
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
4D
HOLD
±30 ADJ
WRITE
READ
A3
A2
A1
A0
GND
4:5/A
BLF
WR
5:6/B
BHF
RD
5D
LS10
CLOCK WEL
CLOCK WEH
CLOCK RE
THIS SHEET -20 ONLY



REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
+5v
R18 10K
R17 10K
7D 38
INTR 6
4:7/D
C10 7-40pf
Y1 32.768 KHZ
C11 10pf
5:3/B V BATT
P4-1
RESET 3:6/A
BRD 4:7/B
BWR 4:7/B
BDEN 5:7/B
P4-10
BDT/R 4:8/B 5:8/C
BM/10 4:7/A
INTR5 4:7/D
INTR7 4:7/D
BA7 4:7/B
BA6
P4-20
BA5
BA4
BA3
BA2
BA1
BA0 4:7/B
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
P4-34
4:8/A 5:8/B BA1-BA6
4:7/C 5:7/C 6:7/C BD0-BD7
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC - PWB
SCALE
SIZE D
PART NUMBER 0114-2011
REV C
CODE
SHEET OF

NOTES: UNLESS OTHERWISE SPECIFIED.

1. TORQUE TO 18 IN. LBS. (DO NOT BREAK INSULATION)

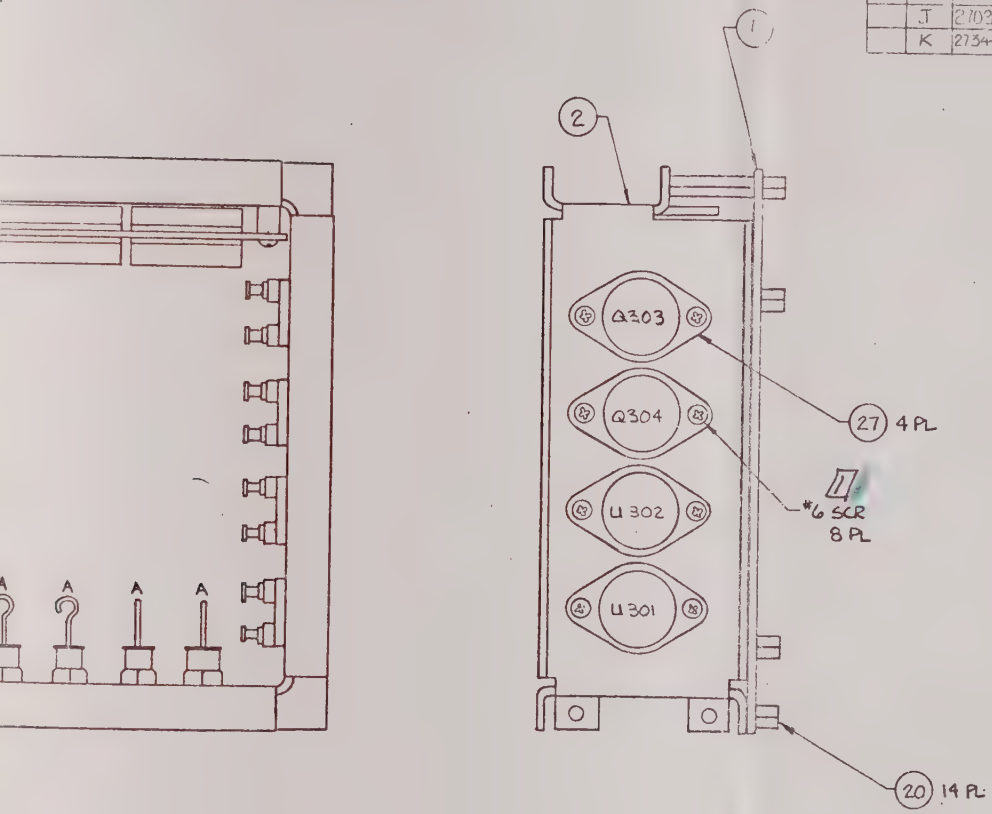
CHASSIS ASSY DETAIL

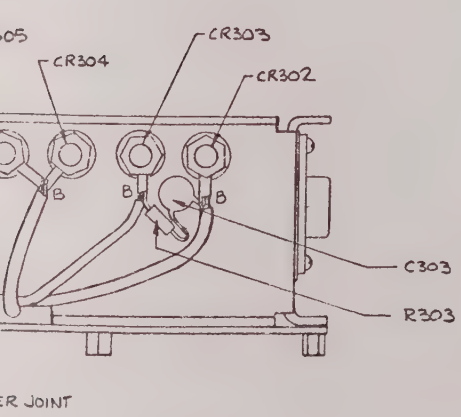
(SEE SHEET 2 FOR COVER ASSY & WIRING)

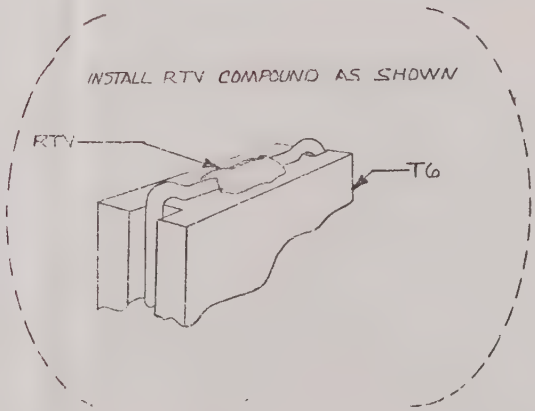
DWG. NO. 0114-0320 | SH 1 | REV K

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B	~	PILOT REL PER ERN 0197	MS	JGH	4/28/81
	C	2236	REVISED PER ECO.	MS	RD	12/4/81
	D	2234	REVISED PER ECO.	MS	JW	1/1/82
	E	2327	REVISED PER ECO #	[illegible]	RD	2/4/82
	F	2519	REVISED PER ECO#	JWC	T.J.	7-6-82
	G	2607	REVISED PER ECO	JWC	T.J.	7/6/82
	H	2649	REV'D PER ECO	[illegible]	[illegible]	
	J	2703	" " "	DGW	[illegible]	
	K	2734	REVISED PER ECO N°	JWC	[illegible]	2-17-88







PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
			1

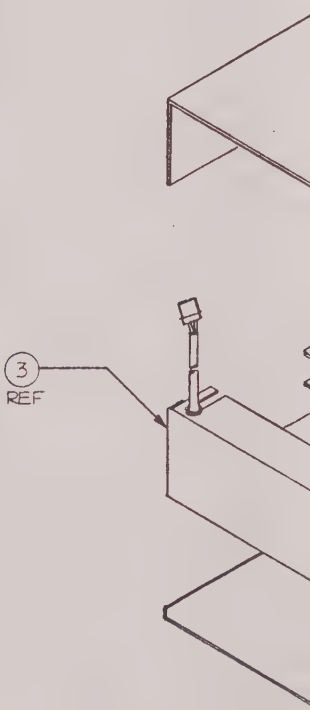
DRAWN | DATE
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR

GOULD biomation

TITLE: TOP ASSY K101/K500 PWR SUPPLY

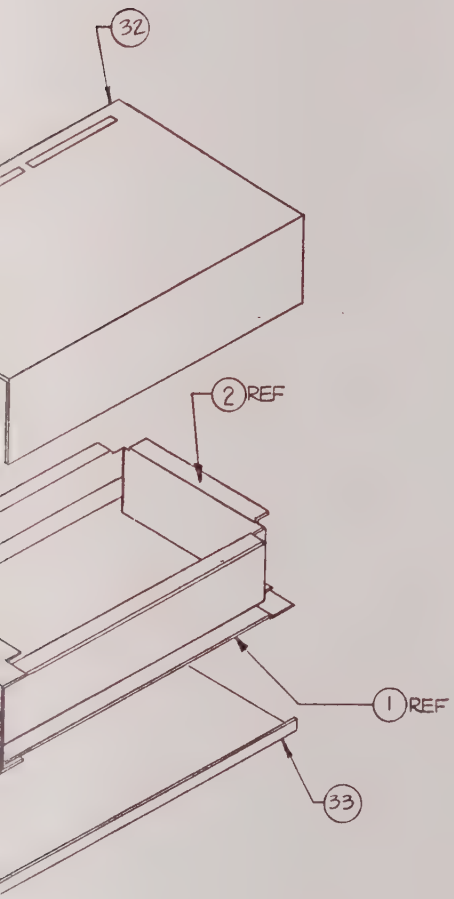
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0320	K

CODE | SHEET 1 OF 2


3
REF

DWG. NO. 0114-0320 | SH 2 | REV 1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



WIRE LIST

WIRE NO.	FROM	TO	DESCRIPTION
1	S3-5	E7 PWR SUPP. PWA	BLU/BLK PART OF
2	S3-8	E8	BLU/BLK ITEM 3
3	S3-4	E9	WHT/BRN
4	S3-7	E10	WHT/BRN
5	S3-1	E14	BLK
6	S3-2	E13 PWR SUPP. PWA	GRY
7	J1-2	E18 PWR SUPP. PWA	WHT/BRN PART OF
8	J1-4	E17 PWR SUPP PWA	BLU/BLK ITEM 3
9	E54 PWR SUPP. PWA	CR301 +	YEL
10	E55	CR301 -	BLK PART OF
11	E6	CR301-R (AC)	ORG ITEM 1
12	E15 PWR SUPP. PWA	CR301-L (AC)	VIO
13			
14			
15			
16			
17	E19 PWR SUPP PWA	C301-	BRN PART OF
18	E20	C301+	RED ITEM 1
19	E21	C302-	BRN
20	E22 PWR SUPP PWA	C302+	RED
21	E36 PWR SUPP PWA E36 PWR SUPP PWA	CR306-A CR307-A	WHT/BLK. SOLDER SAME WIRE 2 PL AS A BRIDGE.
22	E38 PWR SUPP PWA E38 PWR SUPP PWA	CR304-B CR305-B	YEL. SOLDER LUGS & WIRE AS SINGLE JOINT.
23	E40 PWR SUPP PWA E40 PWR SUPP PWA	CR303-A CR302-A	WHT/RED. SOLDER SAME WIRE 2 PL AS A BRIDGE.
24	E14 FILTER PWA	E62 PWR SUPP PWA	BRN
25	E13	E66	RED ITEM 10
26	E12 FILTER PWA	E65 PWR SUPP PWA	ORG
27	E9 FILTER PWA	E41 PWR SUPP PWA	BLK
28	E10	E42	BLK ITEM 9
29	E7	E43	BRN
30	E8	E37	YEL
31	E11 FILTER PWA	E44 PWR SUPP PWA	LT BLU
32	E1 FILTER PWA	E33 PWR SUPP PWA	BRN
33	E2	E30	RED
34	E3	E31	ORG ITEM 11
35	E4	E32	YEL
36	E5	E34	LT BLU
37	E6 FILTER PWA	E35 PWR SUPP PWA	GRN
38	T6 (-2V LEAD)	CR303-B	-2V LEADS ARE EITHER OF TWO FLYING LEADS FROM BOTTOM SIDE OF T6
39	T6 (-2V LEAD)	CR302-B	
40	T6 (-5V LEAD)	CR306-C	-5V LEADS ARE EITHER OF TWO FLYING LEADS FROM TOP SIDE OF T6
41	T6 (-5V LEAD)	CR307-C	
42	FILTER-G	E16	GRN. MTD ON FACE PLATE FILTER
43			
44			
45			
46			

PART OF ITEM 1

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

GOULD biomation

TITLE TOP ASSY K101/K500 POWER SUPPLY

SCALE | SIZE D | PART NUMBER 0114-0320 | REV

CODE

DRAWN | DATE

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSY

ENG SERV

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						
	-00	-[illegible]	-[illegible]	-[illegible]	-[illegible]	-[illegible]	[illegible]
1						1	011[illegible]
2						1	011[illegible]
3						1	011[illegible]
4						1	0114
5							
6							
7							
8							
9						1	0114
10						1	0114
11						1	0114
12							
13						2	140
14						1	1700
15						1	170
16						2	150
17							
18							

DASH NO.	NUMBER	QTY
-10	0950-0003	1
-10	0114-0003	1
	NEXT ASSEMBLY	

DRAWN M. Bu[illegible]

CHECKED J. W[illegible]

ENGINEER

MANUFACTURIN[illegible]

QUALITY ASSU[illegible]

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0090	PWR SUPPLY PWA				LM
-0320	HEATSINK ASSY				LM
-0340	FACE PLATE ASSY				LM
-0360	FILTER PWA				LM
-0366	WIRE ASSY			DIGITAL	LM
-0367	WIRE ASSY			ANALOG	LM
-0368	WIRE ASSY			LED	LM
-0039	TRANSISTOR	Q303, Q304		2N4276	
-0089	IC	U302		LM337K	
-0109	I.C REGULATOR	U301		LM350K	
-0020	TRANSISTOR	Q301, Q302		HPWR6501/HPWR6502	

T DRAWINGS	REV	DESCRIPTION	DATE	DWN	CK'D	APP'D
	A	PROTOTYPE	6-24-81	[illegible]		
	B	PILOT REL PER ECN 0197	7-29-81	[illegible]	[illegible]	
	C	REVISED PER ECO # 2236	10/15/81	[illegible]	[illegible]	
	D	REVISED PER ECO # 2234	11/13/81	[illegible]	[illegible]	
	E	REVISED PER ECO # 2327		[illegible]	[illegible]	
	F	REVISED PER ECO NO 2519	[illegible]	[illegible]	[illegible]	
	G	REVISED PER ECO NO 2607	[illegible]	[illegible]	[illegible]	

	DATE
S	6-26-81
	10-15-81
NCE	

LIST OF MATERIAL
TOP ASSEMBLY
POWER SUPPLY
K101/K500

biomation

B | 0114-0320 | REV K

MODEL K101-K500 | CODE | SHEET 1 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -50	-50	-40	-30	-20	-1	PA
19						2	30
20						1	70
21						2	40
22						4	700
23						1	700
24						1	720
25							
26							
27						4	720
28						2	720
29						1	600
30							
31							
32						1	01
33						1	01
34							
35							
36							

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			CHECKED
			ENGINEER
			MANUFACTURI
			QUALITY ASSU
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]-1206	RESISTOR	R303, 304		12Ω ½W 5%	
[illegible]	SPANDOFF			M/F, HEX, 6-32 x ¼	
[illegible]-0049	CAPACITOR	C303, 304		.01, 1KV, ±20%	
[illegible]-0152	SPACER			#6 × 5/16 LG	
[illegible]-0221	SHOULDER WASHER	@ U1		#4	
[illegible]-0017	INSULATOR	@ U1			
[illegible]-0016-10	INSULATOR	@ Q303 Q304, U301, U302		TO-3	
[illegible]-0016-20	INSULATOR	Q301, 302		TO-3 9MIL	
[illegible]-0329	SHORTING PLUG	@ E24 & E25		2 POSITION	
[illegible]-0327	TOP COVER				FAB
[illegible]-0328	BOTTOM COVER				FAB

[illegible] DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	H	REV'D PER ECO 2649	7-[illegible]	[illegible]	[illegible]	
	J	" " " 2709	9-[illegible]	[illegible]	[illegible]	
	K	REVISED PER ECO NO. 2743	2-[illegible]	[illegible]	[illegible]	

	DATE
	6-26-81
ANCE	

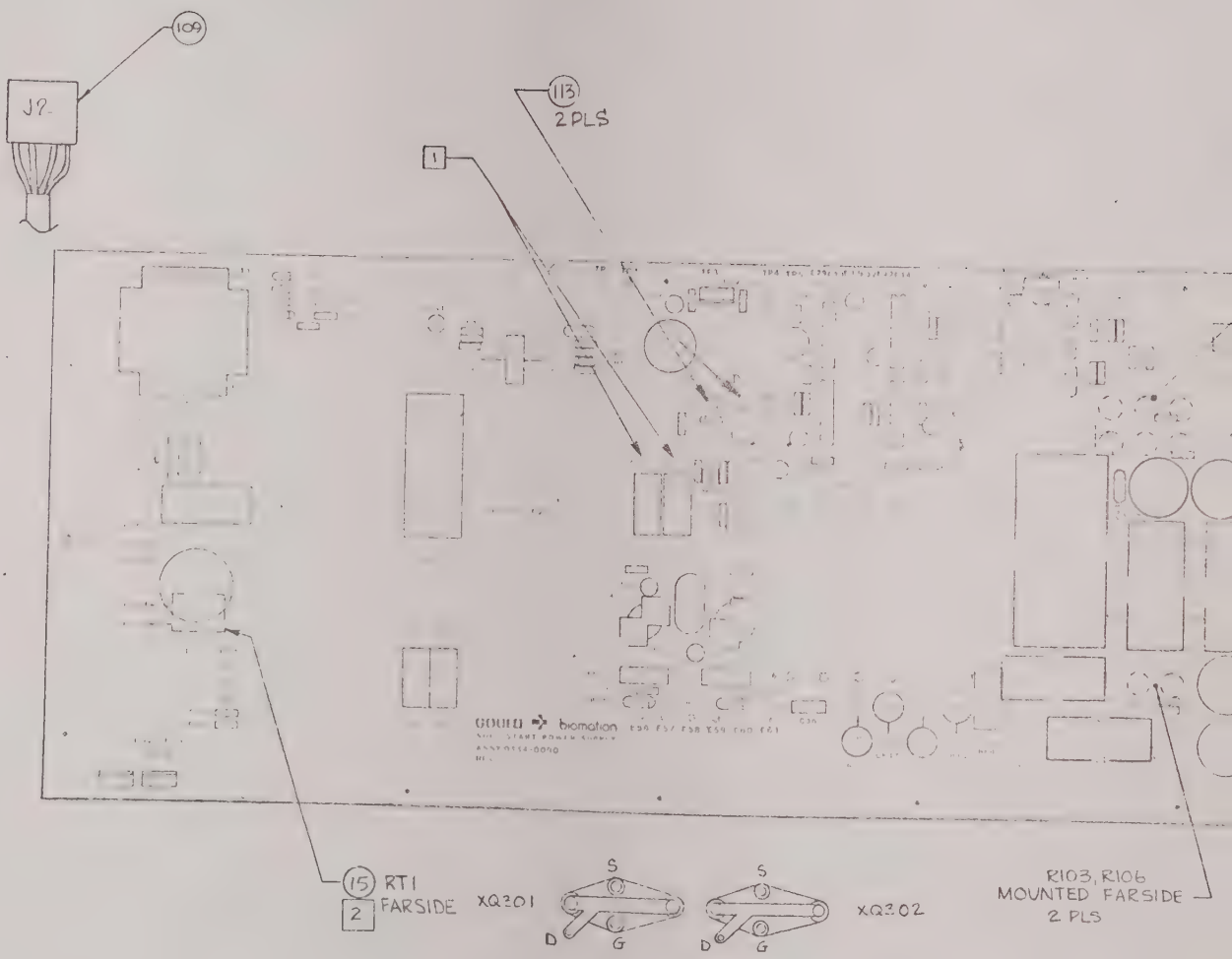
LIST OF MATERIAL

TOP ASSEMBLY
POWER SUPPLY
K101/K500

biomation

B | 0114-0320 | REV K

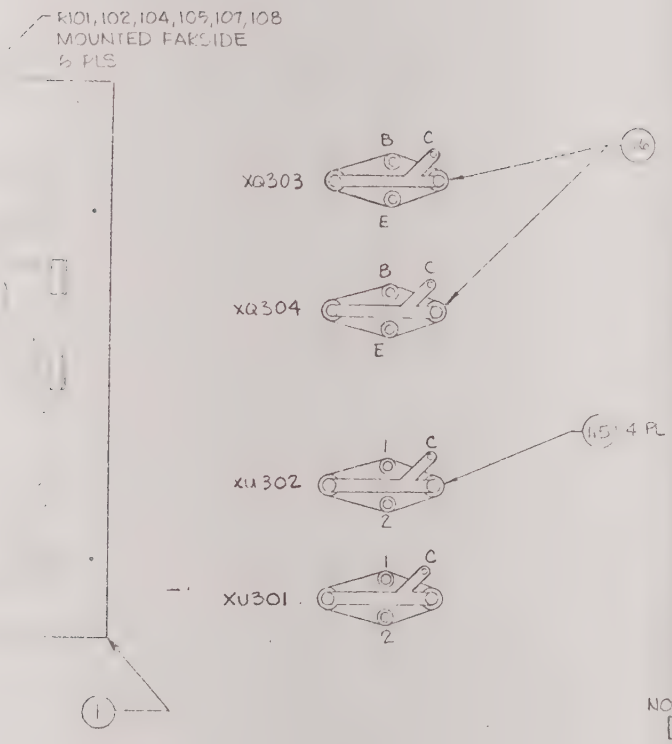
MODEL NOTED | CODE _____ | SHEET 2 OF 2



FROM	TO	COLOR	AUX	REMARKS	ITEM NO
E 46					
47					
E 48					

FROM	TO	COLOR	AUX	REMARKS	ITEM NO
E 36					
E 38					
40					

REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A					
B		[illegible] PER ERN 0191	[illegible]		
[illegible]					
D	2521	REVISED PER ECO	[illegible]	[illegible]	[illegible]
E	2519	REVISED PER ECO Nº	[illegible]	[illegible]	[illegible]
F	[illegible]				
[illegible]					
[illegible]		[illegible] OID			
[illegible]					
[illegible]					
[illegible]					
N		REVISED PER ECO Nº	DGW	[illegible]	
M	3515	REVISED PER ECO Nº	SWC	DGW	[illegible]
P	3576A	REVISED PER ECO Nº	MW	DGW	[illegible]
R	3734	REVISED PER ECO	MW	DGW	[illegible]



NOTES:

1. R8, R9 ARE TO BE MOUNTED WITH 1/4" CLEARANCE BETWEEN RESISTOR BODY AND PCB.
2. WRAP BODY OF RT1 WITH KAPTON TAPE. INSTALL ON SOLDER SIDE FLUSH AGAINST PCB.

DRAWN	DATE	GOULD biomation	
CHECKED		TITLE ASSY PCB [illegible]	
PROJ. ENG.			
MANUFACTURING		SCALE / SIZE D / PART NUMBER [illegible]	REV P
QUALITY ASSUR			

COMMENTS		TOTAL COST	UNIT COST

SSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PAR
	-60	-50	-40	-30	-20	10	
1						1	2[illegible]
2							
3						4	1000-
4							
5						2	1100
6						4	1200-
7						1	1100-
8						4	1200-
9							
10							
11						2	1500-
12							
13						2	1400-
14						1	1400-
15						2	3600
16						1	1700-
17							
18						2	1700-
							RE

			DRAWN J.W.
			CHECKED
			ENGINEER
			MANUFACTURING
-10	0114-03[illegible]	1	QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	PWB				[illegible]
[illegible]	DIODE	[illegible]		IN4152	
[illegible]0046	" "	CR 14 & 15		P6KE22A	
[illegible]0001	" "	CR 1-4		IN4002	
[illegible]0056	" "	CR7		IN758A	
[illegible]0042	RECTIFIER	CR16, 17, 18, 19		MR821	
[illegible]	TRANSISTOR	Q 2 & 3		2N3904	
[illegible]	TRANSISTOR	Q4, 5		2N6134	
[illegible]19	TRANSISTOR	Q1		2N3906	
[illegible]	THERMISTOR	RT 1 & 2			
[illegible]	IC	U1		LM 340T-15	
[illegible]	IC	U5 & [illegible]		LM 324	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	B	PILOT [illegible] 0197	[illegible]	[illegible]	[illegible]	
	C	REVISED [illegible] ECO # 2634	[illegible]	[illegible]	[illegible]	[illegible]
	D	REVISED PER ECO # 2421	[illegible]	[illegible]	[illegible]	
	E	REVISED PER F[illegible] 2519	[illegible]	[illegible]	[illegible]	
	F	REVISED PER [illegible] # 2563	[illegible]	[illegible]	[illegible]	
	G	" " 2634	[illegible]	[illegible]	[illegible]	
	H	- VOID - [illegible] 2[illegible]	[illegible]	[illegible]	[illegible]	

DATE
[illegible]
[illegible]

LIST OF MATERIAL

PW [illegible]
SOFT START POWER SUPPLY

biomation

B | [illegible] | REV R

MODEL | CODE | SHEET 1 OF 7

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PAR
	-60	-50	-40	-30	-20	-10	
20						1	13
21						1	
22						1	1700
23						1	3000
24						10	3000
25						3	3000
26						3	3000
27						2	3000
28						3	3000
29						1	3000
30						1	3100
31						4	3000
32						1	3000
33						2	3000
34						1	3000
35						1	3100
36						4	

			DRAWN
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			QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	IC	U4		74C174	
[illegible]	IC	U3		14025	
[illegible]	IC	U7,8		[illegible]	
[illegible]	IC	U2		71494	
[illegible]	RESISTOR	R109		470Ω, 1/4W, 5%	
[illegible]	RESISTOR	R4, 10, 15, 16, 17, 25, 29, 37, 41, [illegible]		10K 1/4W 5%	
[illegible]	RES	R2, 3, 13, 18, 19, 20, 22, [illegible]		100K	
[illegible]	RES	R40, 53, 55		220Ω	
[illegible]	RES	R61 & 64		20Ω	
[illegible]	RES	R63, 66		390Ω	
[illegible]	RES	R30		13K 1/4W, 5%	
[illegible]	RES	R11		18.7K 1/8W, 1%	
[illegible]	RES	R5, 32, 33, 34		6.2K 1/4W, 5%	
[illegible]	RES	R74		47Ω 1/4W, 5%	
[illegible]	RES	R7, 38		4.7K 1/4W, 5%	
[illegible]	RES	R44		5.6K 1/4W, 5%	
[illegible]002	RES	R12		20K 1/8W, 1%	
[illegible]	RES	R28, 31, 46, 48		3.1K 1/4W 5%	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	J	REVISED PER ECO 2709	9-8-82	DGW	[illegible]	
	K	" " " 2717	[illegible]	[illegible]	[illegible]	
	L	" " " 2741	[illegible]	[illegible]	[illegible]	
	M	" " " 2738	[illegible]	[illegible]	[illegible]	
	N	REVISED PER ECO No 3575	8-10-[illegible]	[illegible]	[illegible]	
	P	REVISED PER ECO No 3575A	[illegible]	[illegible]	[illegible]	[illegible]
	R	REVISED PER ECO 3734	[illegible]	[illegible]	[illegible]	[illegible]

DATE	LIST OF MATERIAL	biomation
	PW ASSEMBLY SOFT START POWER SUPPLY	B D114-0090 REV R
	MODEL	CODE SHEET 2 OF 7

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PAR
37						1	300
38							
39						1	3
40						1	3150
41						1	
42						2	30
43						1	
44						2	307
45						1	3050
46						2	
47						2	
48						1	30
49						1	
50						1	30
51						1	307
52						1	307
53						2	
54						1	

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-1201	RES	R110		12K, 1/4W, 5%	
				15K 1/4W 5%	
	RES	R26		150K 1/4W 5%	
-1542	RES	R14		29.4K 1% 1/4W	
01	RES	R42		9.1K 1/4W 5%	
02	RES	21, 75		20K 1/4W 5%	
03	RES	R37		120K 1/4W 5%	
-00	RES	R62, 65		470Ω 1W 5%	
-3306-10	RES	R6		33Ω 1/2W 5%	
-01	RES	R70, 71		1.50K 1/8W 1%	
-1500	RES	R72, 73		150Ω 1/8W 1%	
-2706	RESISTOR	R49		27Ω 2W	
	RESISTOR	R68		51Ω 2W	
	RESISTOR	R52		20Ω 1/2W	
	RESISTOR	R35		82Ω 1/2W 5%	
-1067	RESISTOR	R56		1Ω 1/2W	
-1540	RESISTOR	R59, 60		56K 2W 5%	
	RESISTOR	R58		22Ω 2W	

	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE
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LIST OF MATERIAL

PW ASSEMBLY

SOFT START POWER SUPPLY

biomation

	MODEL	B	C114-0090	REV K
		CODE		SHEET 2 OF 7

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART
57						5	340
58						2	
59						2	
59						1	3700
59						1	3700
60						1	4000
61						1	0114-
62						1	0114-
63						1	0114-
64						1	4300
65						2	4000
66						2	4000
67						1	4100
68						7	
69						2	
70						7	
71						1	
72						1	

			REF

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURAN
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	[illegible]	R101, 102, 103, 106, 108		200 Ω, 1/2W, 10%	
[illegible]	[illegible]	[illegible]		[illegible]	
[illegible]	RESISTOR	R8, 9		300 Ω [illegible]	
[illegible]	RESISTOR PAK	RP1		100K 8 PIN	
[illegible]	RESISTOR PAK	RP2		4.7K 8 PIN	
[illegible]	CAPACITOR	C4		.1 uf, 100V	
[illegible]	RESISTOR COIL	R50		3 mΩ	
[illegible]	RESISTOR COIL	R51		1.9 mΩ	
[illegible]	RESISTOR COIL	R43		1.2 mΩ	
[illegible]	CAPACITOR	C15		100uf 20V	
[illegible]	CAPACITOR	C1, C2		.01 UF, 3KV, 20%	
[illegible]	CAPACITOR	C5, 28		.01uf, [illegible], 20%	
[illegible]	CAPACITOR	C33		330 [illegible], [illegible], 5%	
[illegible]	CAPACITOR	C7, 8, [illegible], [illegible], [illegible], [illegible]		.1uf, 50V, 20%	
[illegible]	CAPACITOR	C41, 42		1.0, 35V, 20%	
[illegible]	CAPACITOR	C3, 14, 19, [illegible], 25, [illegible], 26		.1uf 50V, 10%	
[illegible]	CAPACITOR	C21		330 Pf, 500V, 5%	
[illegible]	CAPACITOR	C45		22 uf 450V	

[illegible]NGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

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LIST OF MATERIAL

PW ASSEMBLY

SOFT START POWER SUPPLY

biomation

B | 0114-0050 | REV R

MODEL | CODE | SHEET [illegible] OF

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PAR
73						1	400
74						1	41
75						1	4
76						5	430
77						3	4400
78						3	4300
79						2	4400
80						1	4200
81						1	900
82						1	4
83						1	9000
84						1	2500
87						1	9000
86						1	9
87						1	9
88						2	9000
89						1	9000
90						2	9
							R

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]-0050	CAP	C36		.005uf, 500V	
[illegible]	[illegible]	[illegible]		[illegible]	
[illegible]	CAP	[illegible]		[illegible] uf 35V	
[illegible]	CAP	[illegible]		4.7uF [illegible]	
[illegible]	CAP	C29, [illegible]		1000uf 15V	
[illegible]	CAP	C6, 13, 34		15 uf, 20 V	
[illegible]2	CAP	C37, 38		470 uf 50V	
[illegible]-0036	CAP	C44		6µf 200V	
[illegible]	ASSY OUTPUT INDUCTOR #2	L5		45 uH (+6V)	LM
[illegible]	NEON LAMP	DS1		NE2	
[illegible]0110	ASSY MAIN TRANSFORMER	T6		"SOFT START"	LM
[illegible]-20	TRANSFORMER	T1		LINE 110/220 P21	
[illegible]	ASSY INPUT TRANSFORMER	T3		BALUN INPUT	LM
[illegible]0078	ASSY TRANSFORMER	T2		CURRENT SENSING XFMR	LM
[illegible]	ASSY OUTPUT INDUCTOR	L4		45uH [illegible]	LM
[illegible]0107	ASSY OUTPUT INDUCTOR #1	L2, 3		250µH (± 17v)	LM
[illegible]0111	ASSY OUTPUT INDUCTOR #3	L1		20µH (-5.2v)	
[illegible]0109	TRANSFORMER	T4,5		[illegible]	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE

LIST OF MATERIAL

PW ASSEMBLY
SOFT START [illegible] SUPPLY

biomation

B | [illegible] | REV [illegible]

MODEL | CODE | SHEET [illegible] OF [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PART
	-60	-50	-40	-30	-20	-10	
91						AR	7150-
92							7-
93							7150-
94							7150-
95							7150-
96							7150-
97							7150-
98							7150-
99							7150-
100						V	7150-
101						AR	7150-
102						2	0114-
103						2	0114-
104						1	0114-
105						1	0114-
106						1	0114-
107						1	0114-
108						AR	7150-
							REV

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURAN
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	WIRE			BRN 12 AWG	—
				WHT 12 AWG	—
				ORN 18 AWG	—
				WHT/RED 12 AWG	—
-04				YEL 12 AWG	—
-14				WHT/BLK 12 AWG	—
-04				YEL 18 AWG	—
-02				RED 18 AWG	—
-07				VIO 18 AWG	
3-06				BLU 18 AWG	
08	WIRE			GRY 18 AWG	
	CAP CABLE ASSY			BRN	LM
	" "			RED	LM
-10	ASSY, BRIDLE WIRE			ORG	LM
0545-20	" "			YEL	LM
0545-30	" "			VIO	LM
0545-40	" "			BLK	LM
-02	WIRE			ORG 12 AWG	

REVISIONS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DATE

LIST OF MATERIAL

PW ASSEMBLY

SOFT START POWER SUPPLY

biomation

B

REV R

MODEL

CODE

SHEET OF 7

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PART
	-60	-50	-40	-30	-20	-10	
110						1	[illegible]
111						AR	7[illegible]
112						AR	780-[illegible]
113						2	6000
114						1	4010
115						4	6100
116						2	6100
117							
118							
119						A/R	7200
120						A/R	7100
121						1	4010
122							
123							
124							
125							
126							

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	CABLE ASSY FAN	J2		[illegible]	[illegible]
[illegible]	WIRE			RED 12 AWG	
[illegible]	↓			BLUE 12 AWG	
[illegible]	WIRE			BRN 12 AWG	
[illegible]18	HEADER			3 PIN	
[illegible]03	CAP.	C27		.01uf 50V 10%	
[illegible]49	SOCKET	XQ301, XQ302 XU301, XU302		TO3 MOUNTING WITH .040 TERMINALS	
[illegible]50	SOCKET	XQ303, XQ304		TO3 MOUNTING WITH .060 TERMINALS	
[illegible]46	TEFLON TUBING	T2		20 AWG	
[illegible]39	WIRE	T2		20 AWG	
[illegible]0563	CAP	C10		.056uF 50v 10%	

F. [illegible]INGS	REV	DESCRIPTION	DATE	DWN	CKD	APP'D

	DATE
NCE	

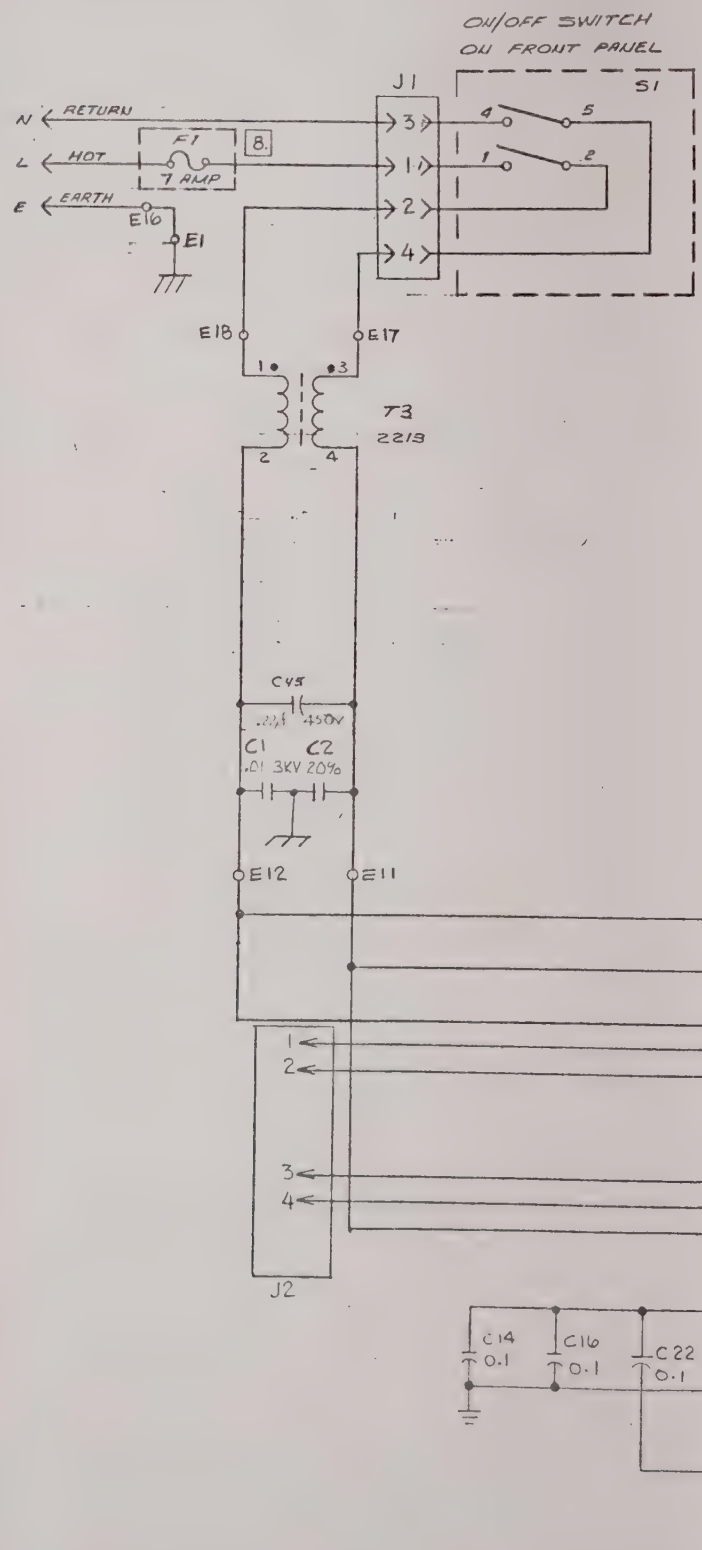
LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

biomation

B | [illegible] | REV R

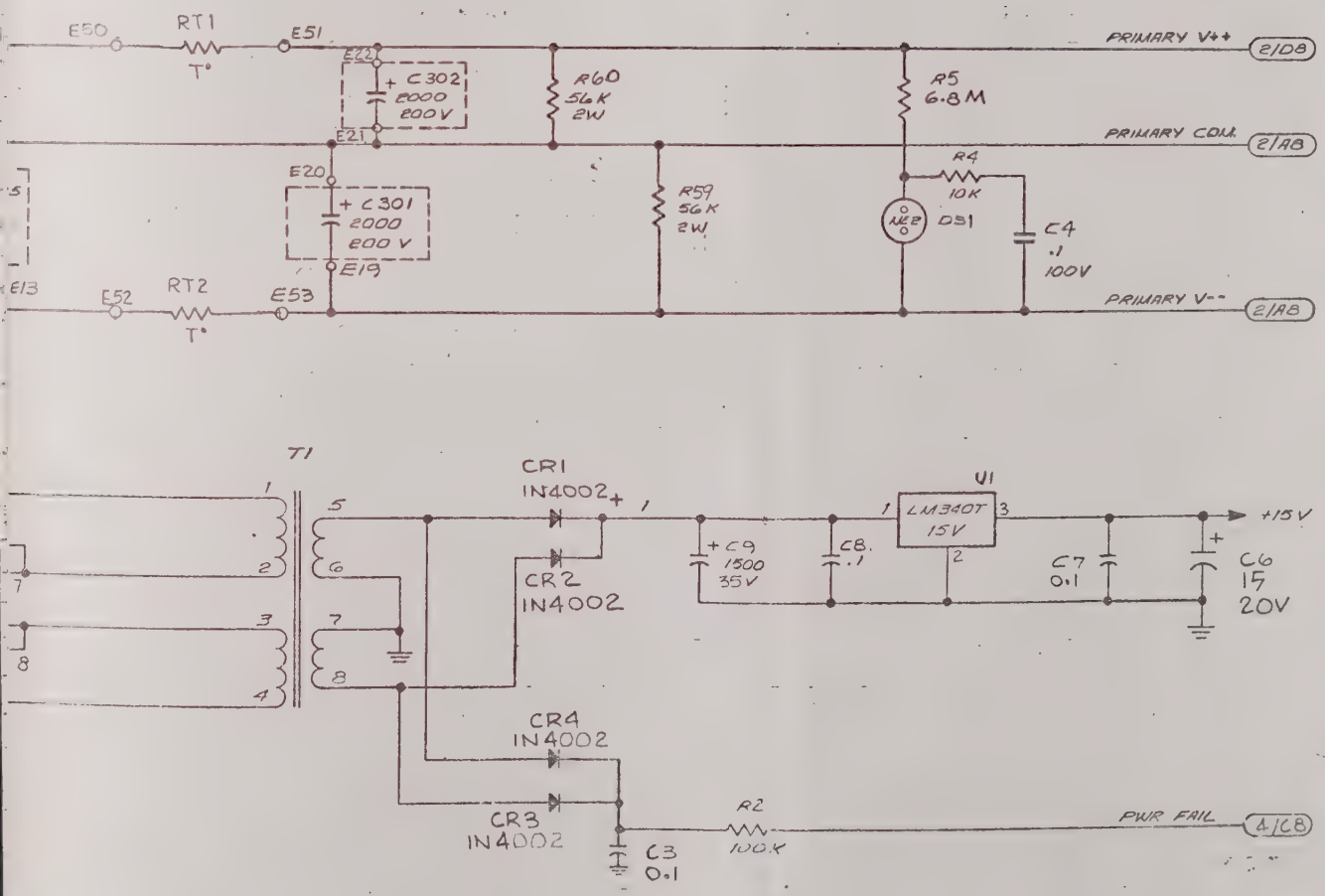
MODEL | CODE | SHEET 7 OF 7



NOTES: UNLES
1. ALL RESISTO
2. ALL CAPACIT
3. ANALOG G
4. DIGITAL GR
5. CHASSIS GA
6. POTS ARE
7. THIS COMPON
8. THIS COMPONE
9. THIS COMPONE

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTOTYPE	JKP		6/4/81
	B		PROD REL PER ERN#0197	RG	RG	9/22/81
	C		INCORPORATED ECO # 2234	JGH	[illegible]	12/8/81
	D	[illegible]	REV'D PER ECO	[illegible]	[illegible]	
	E	[illegible]	REV'D PER ECO	[illegible]	[illegible]	
	F	[illegible]	REV'D PER ECO	[illegible]	[illegible]	
	G	2666	-VOID-	DGW	[illegible]	
	H	2109	REV'D PER ECO	DGW	[illegible]	
	J	2717	" " "	DGW	[illegible]	
	K	3515	REV'D PER ECO	[illegible]	3/10/83	DGW
	—	—	SKIPPED REVISIONS L,M,N	[illegible]		
	P	3578A	REVISED PER ECO	[illegible]	[illegible]	3/21
	R	3134	REVISED PER ECO	MW	DGW	4/1/84

OTHERWISE SPECIFIED
[illegible] ARE IN OHMS, 1/4 W, 5%
[illegible] VALUES ARE IN MICRO FARADS
[illegible] E62
[illegible] E41, E42
[illegible] E16
[illegible]N SOLDER SIDE OF BOARD
[illegible]NT IS ON HEAT SINK ASSY 0114-0330
[illegible]T IS ON FACE PLATE ASSY 0114-340
[illegible]T IS ON TOP ASSY 0114-0320



REF. DES. HIGHEST USED (MAIN PWR ONLY)
R74, C45, Q5, CR19 U8, E70

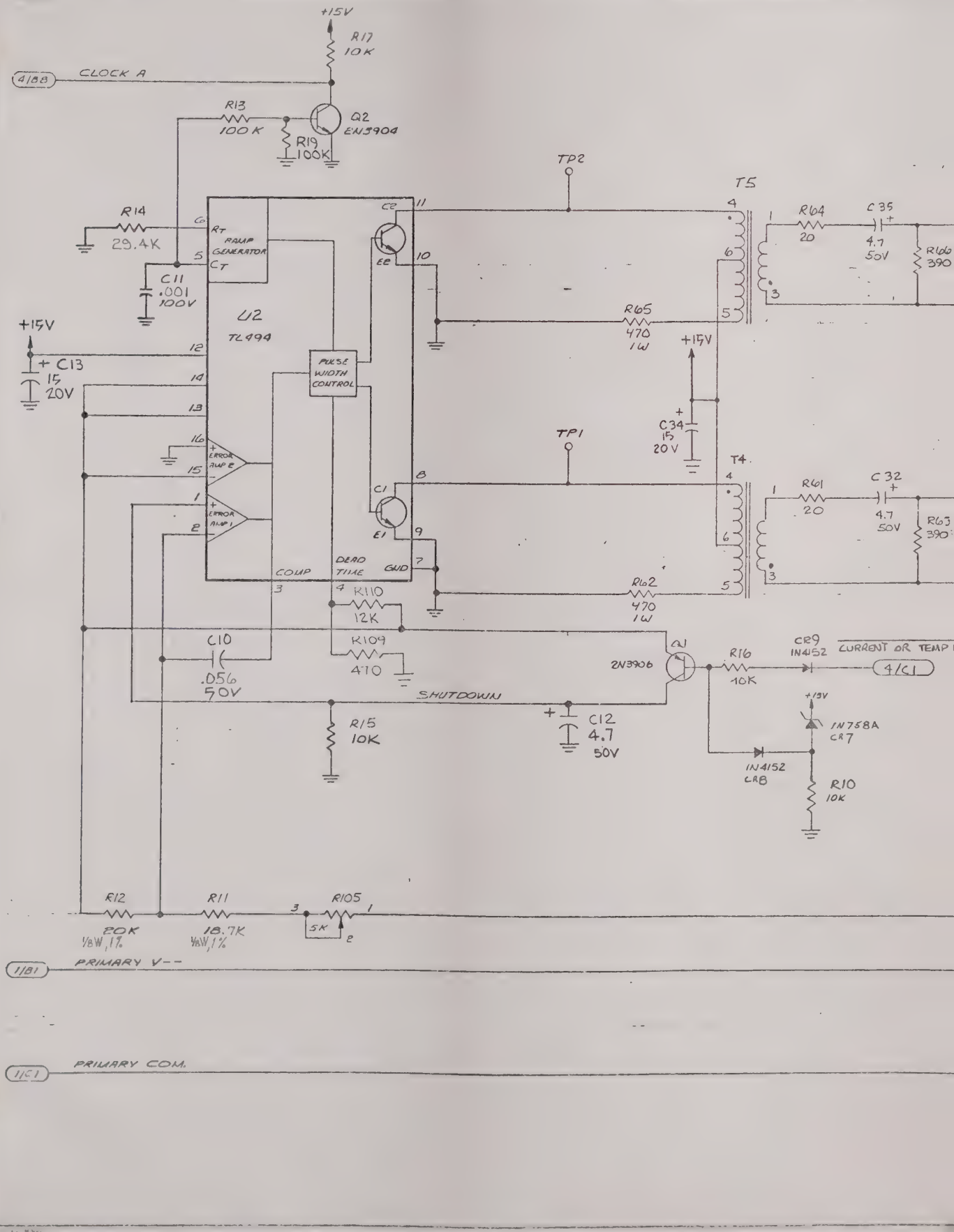
PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

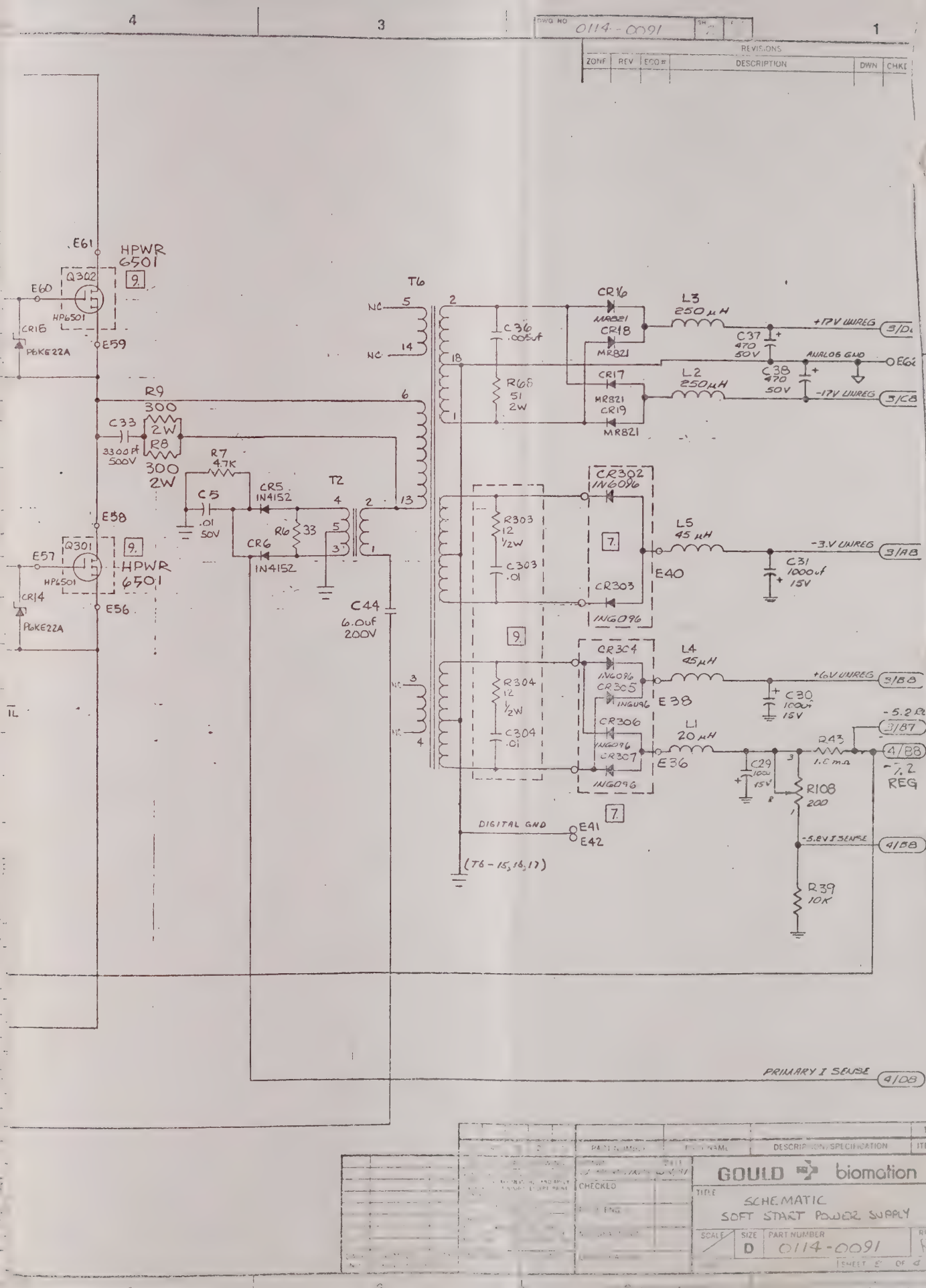
DRAWN J. PERGIAIS DATE 6/4/81
CHECKED [illegible] 9/22/81
QUALITY ASSUR

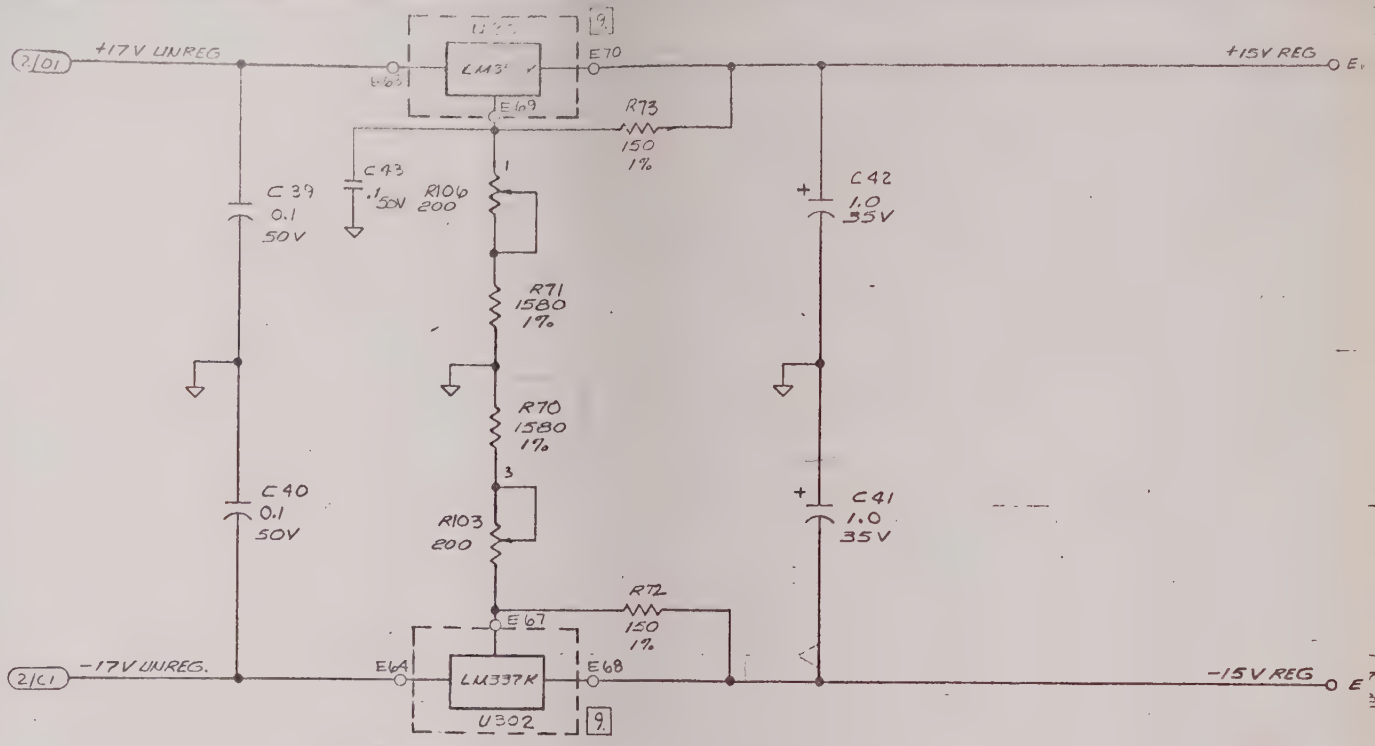
GOULD biomation

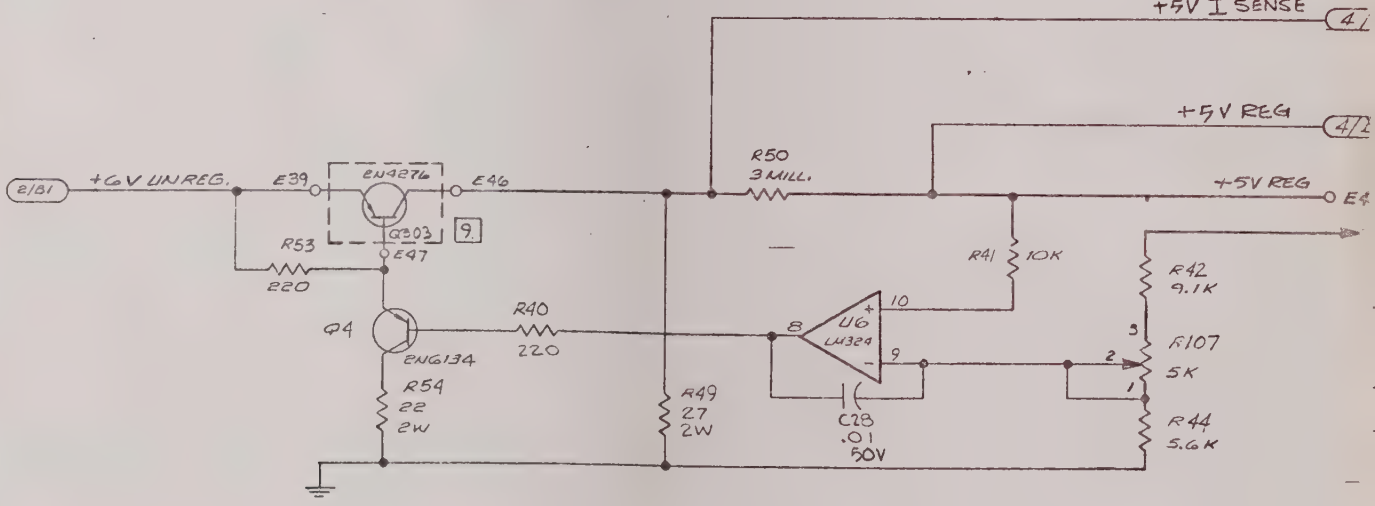
TITLE SCHEMATIC
SOFT START POWER SUPPLY

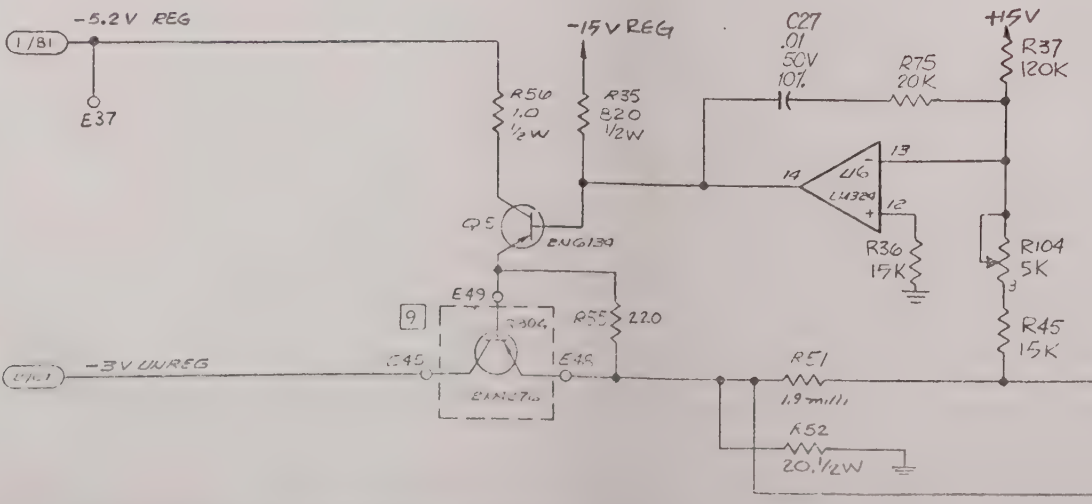
SIZE D PART NUMBER 0114-0091 REV K


8
7
6
5
1/C1
PRIMARY V++
+15V
R17
10K
4/B8
CLOCK A
R13
100K
Q2
2N3904
R19
100K
TP2
T5
R14
29.4K
C2
11
4
R64
20
C35
4.7
50V
R66
390
RT
RAMP GENERATOR
CT
E2
10
6
5
3
C11
.001
100V
U2
TL494
R65
470
1W
+15V
+15V
C13
15
20V
12
14
13
PULSE WIDTH CONTROL
+15V
C34
15
20V
TP1
T4
16
15
ERROR AMP 2
C1
8
4
R61
20
C32
4.7
50V
R63
390
1
2
ERROR AMP 1
E1
9
6
3
5
COMP
DEAD TIME
GND
7
3
4
R110
12K
R62
470
1W
C10
.056
50V
R109
470
Q1
2N3906
R16
10K
CR9
IN4152
CURRENT OR TEMP
4/C1
SHUTDOWN
R15
10K
C12
4.7
50V
+13V
IN758A
CR7
IN4152
CR8
R10
10K
R12
20K
1/8W, 1%
R11
18.7K
1/8W, 1%
3
R105
5K
1
2
1/B1
PRIMARY V--
1/C1
PRIMARY COM.


DWG NO 0114-0091
REVISIONS
ZONE REV ECO # DESCRIPTION DWN CHKD
E61
HPWR 6501
9.
Q302
HP6501
E60
CR15
P6KE22A
E59
R9
300 2W
C33
3300 pf 500V
R8
300 2W
R7 4.7K
C5 .01 50V
CR5 IN4152
T2
R6 33
CR6 IN4152
E58
Q301
HP6501
E57
CR14
P6KE22A
E56
C44 6.0uf 200V
T6
NC 5
NC 14
2
18
1
6
13
4
3
NC 3
NC 4
C36 .005uf
R68 51 2W
CR16 MR821
CR18 MR821
CR17 MR821
CR19 MR821
L3 250 µH
L2 250µH
C37 470 50V
C38 470 50V
+17V UNREG
3/D6
ANALOG GND
E62
-17V UNREG
3/C8
CR302 IN6096
R303 12 1/2W
C303 .01
7.
CR303 IN6096
E40
L5 45 µH
-3.V UNREG
3/A8
C31 1000uf 15V
9.
CR304 IN6096
CR305 IN6096
R304 12 1/2W
C304 .01
CR306 IN6096
CR307 IN6096
E38
L4 45µH
+6V UNREG
3/B8
C30 1000uf 15V
E36
L1 20 µH
R43 1.0 mΩ
-5.2 R
3/B7
4/B8
-5.2 REG
C29 1000uf 15V
R108 200
-5.8V I SENSE
4/B8
R39 10K
DIGITAL GND
E41
E42
(T6-15,16,17)
PRIMARY I SENSE
4/D8
DESCRIPTION/SPECIFICATION
CHECKED
GOULD biomation
SCHEMATIC
SOFT START POWER SUPPLY
SIZE D
PART NUMBER 0114-0091
REV R
SHEET 2 OF 4


+17V UNREG
LM337
E70
+15V REG
E69
R73
150
1%
C43
.1
50V
R106
200
C39
0.1
50V
C42
1.0
35V
R71
1580
1%
R70
1580
1%
C40
0.1
50V
R103
200
C41
1.0
35V
R72
150
1%
E67
-17V UNREG.
E66
LM337K
E68
-15V REG
U302


+5V I SENSE
+5V REG
+6V UNREG.
E39
ENG276
E46
Q303
R50
3 MILL.
+5V REG
R53
220
E47
R41
10K
R42
9.1K
Q4
ENG134
R40
220
U6
LM324
R107
5K
R54
22
2W
R49
27
2W
C28
.01
50V
R44
5.6K

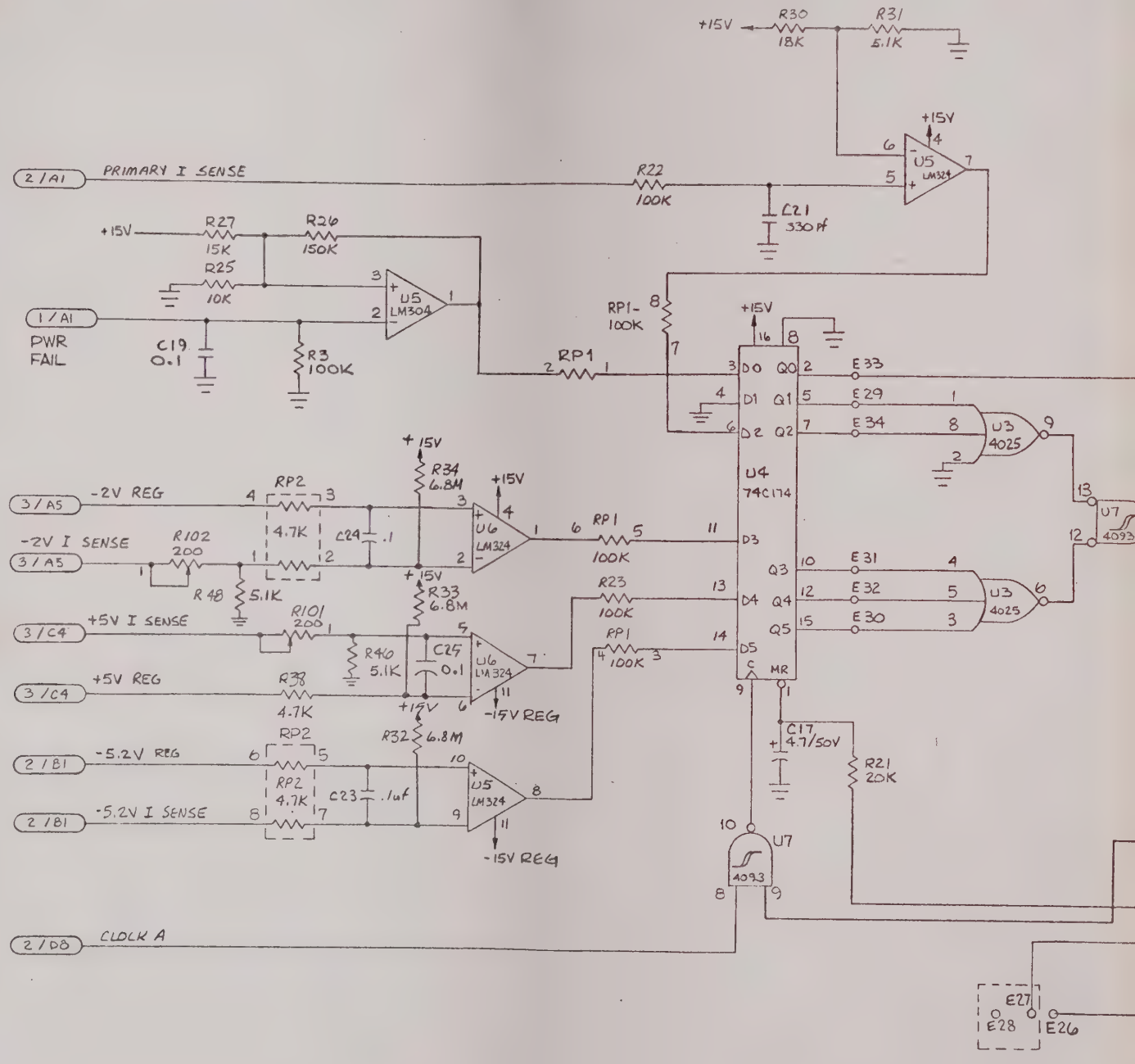

-5.2V REG
E37
-15V REG
C27
.01
50V
10%
R75
20K
+15V
R37
120K
R50
1.0
1/2W
R35
820
1/2W
U6
LM324
Q5
ENG139
R36
15K
R104
5K
R45
15K
E49
R55
220
-3V UNREG
E48
R51
1.9 mill
-2V REG
R52
20. 1/2W
-2V I SENSE

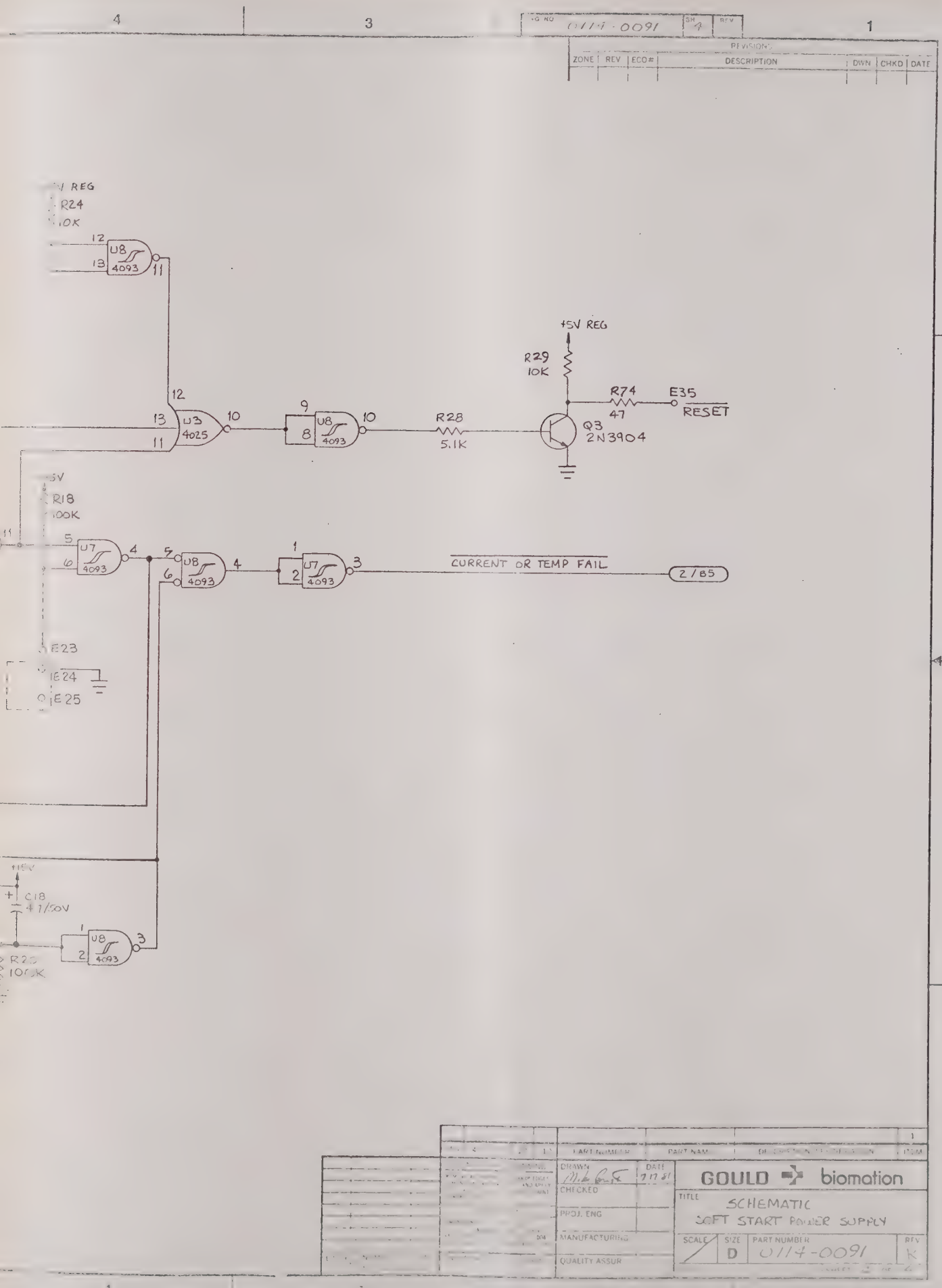
REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DRAWN J. FERGINS	DATE 6/4/81	GOULD biomation
CHECKED		TITLE SCHEMATIC SOFT START POWER SUPPLY
PROJ ENG		
MANUFACTURING		SCALE / SIZE D PART NUMBER C114-C091 REV
QUALITY ASSUR		SHEET OF

DASH NO | NUMBER | QTY | NEXT ASSEMBLY | ENG SERV | DATE


+15V
R30
18K
R31
5.1K
U5
LM324
2/A1
PRIMARY I SENSE
R22
100K
C21
330 pf
R27
15K
R26
150K
R25
10K
U5
LM304
1/A1
PWR
FAIL
C19
0.1
R3
100K
RP1-
100K
RP1
U4
74C174
E33
E29
E34
U3
4025
U7
4093
3/A5
-2V REG
RP2
4.7K
C24
.1
U6
LM324
-2V I SENSE
R102
200
R48
5.1K
R34
6.8M
R33
6.8M
R23
100K
3/C4
+5V I SENSE
R101
200
R40
5.1K
C25
0.1
+5V REG
R38
4.7K
-15V REG
2/B1
-5.2V REG
-5.2V I SENSE
R32
6.8M
C23
.1uf
C17
4.7/50V
R21
20K
2/D8
CLOCK A
E27
E28
E26



0114-0091
SH 4
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
REG
R24
10K
U8
4093
U3
4025
+5V REG
R29
10K
R74
47
E35
RESET
R28
5.1K
Q3
2N3904
R18
100K
U7
4093
CURRENT OR TEMP FAIL
2/B5
E23
E24
E25
C18
47/50V
R20
100K
PART NUMBER
PART NAME
DESCRIPTION
ITEM
DRAWN
DATE
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
SCHEMATIC
SOFT START POWER SUPPLY
SCALE
SIZE
D
PART NUMBER
0114-0091
REV
K

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PAR
1					1	1	011
2							
3					1	1	120
4							
5					1	1	0114
6					1	1	0114
7					1	1	6000
8					1	1	7300
9					1	1	7300
10					AR	AR	
11					—	1	7300
12					1	—	7300
13							
14					1	1	6700
15					AR	AR	7150-
16					A/R	A/R	7150-
17							
18							

			DRAWN MLS
			CHECKED
			ENGINEER
			MANUFACTURING
-10	0114-0820	1	QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	FACE PLATE				FP
[illegible]034	RECTIFIER BRIDGE	CR301	MDA3504	400V 30A	
[illegible]043	WIRE ASSY			POWER CABLE	LM
[illegible]042	WIRE ASSY			LINE VOLTAGE SELECT	LM
[illegible]47	PWR LINE FILTER				
[illegible]2018	FUSE HOLDER SOCKET	XF1			
[illegible]2019	BAYONNET CAP				
	WIRE, BUSS			22 AWG	
[illegible]-0029		F1		7A-3AG-125 V	
[illegible]-0030-10		F1		4A-3AG-250V	
[illegible]-0035	SWITCH, SLIDE	S3		3PDT	
[illegible]-05	WIRE			18 AWG GRN	
[illegible]2018-01	WIRE			18AWG BRN	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PROTOTYPE	6 26 81	[illegible]		
	B	PILOT REL PER ERN 0197	9/[illegible]/81	RG	JGH	9/29/81

	DATE
[illegible]	6 26 81
[illegible]	10-[illegible]-81
NCE	

LIST OF MATERIAL

FACE PLATE ASSY
POWER SUPPLY

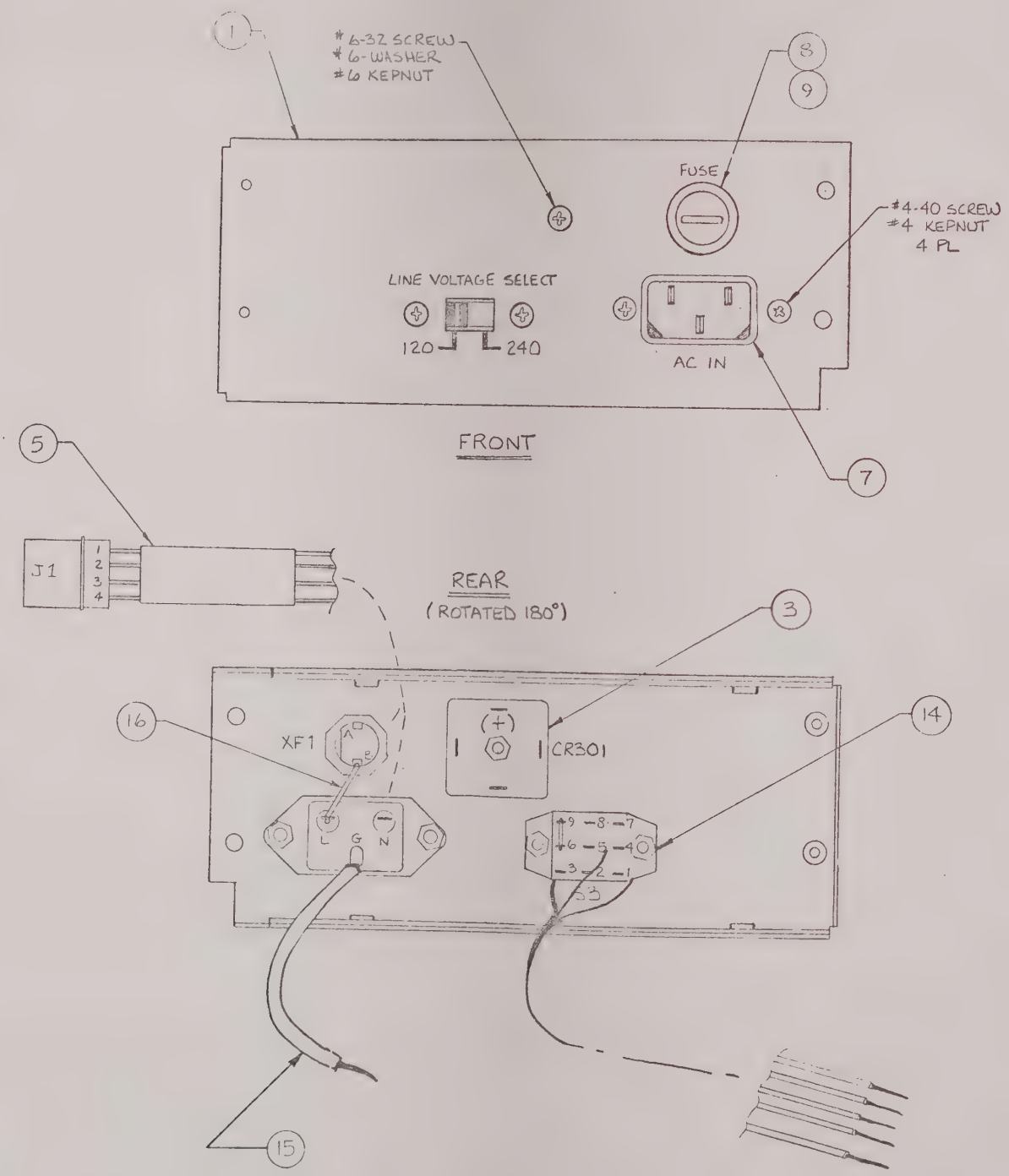
biomation

B	0114-0340	REV B

MODEL

CODE

SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED,

1. SLEEVE CONNECTIONS AS REQD.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	-	PROTOTYPE	MB		
	B		PILOT REL PER ERN 0197	R	JGH	9/29/81

WIRING LIST

FROM	TO	COLOR		REMARKS
XF1-B	FILTER-L	BRN		ITEM 16
J1-1	XF1-A	WHT/BRN		ITEM 5
J1-3	FILTER-N	BLU/BLK		
J1-2	N.C.	WHT/BRN		
J1-4	N.C.	BLU/BLK		
S3-6	S3-9	BUSS		ITEM 10
S3-5	N.C.	BLU/BLK		ITEM 6
S3-8		BLU/BLK		
S3-4		WHT/BRN		
S3-7		WHT/BRN		
S3-1		BLK		
S3-2		GRY		
FILTER-G		GRN		ITEM 15

DWG. NO. 0114-0340

SH 1

REV. B

40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
							1

DO NOT SCALE DRAWING

...VE ALL BURRS AND SHARP EDGES ...SIONS ARE IN INCHES AND APPLY ... ADDED FINISHES EXCEPT PAINT ...FACE ROUGHNESS

TOLERANCE

MENSIONAL	HOLE SIZE
1 ANGLES	0 599 · 003
X · 020 1	600 999 · 004
XX · 010	1 000 1 499 · .005

NG. SERV.	DATE

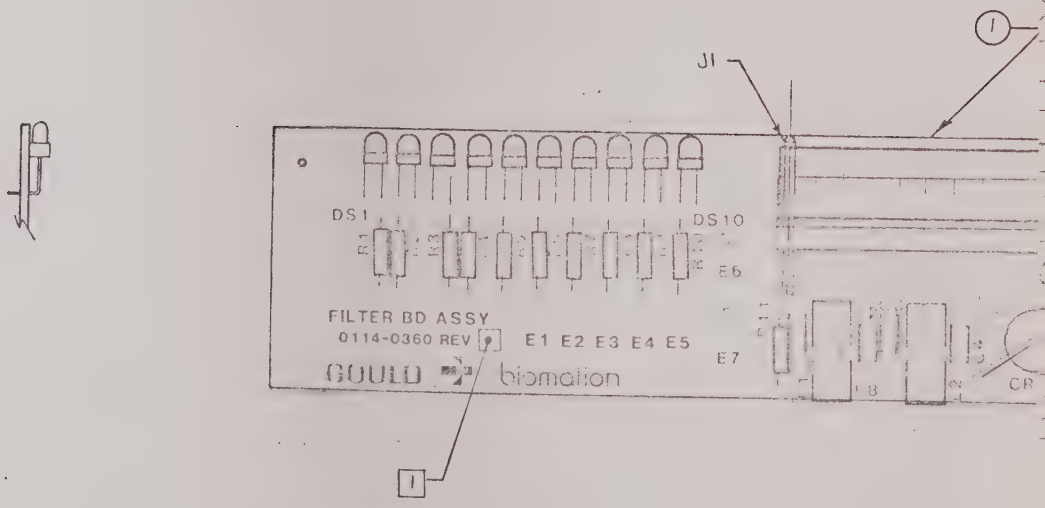
DRAWN	DATE	
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		

GOULD biomation

TITLE: FACE PLATE ASSY, PUR SUPPLY

SCALE	SIZE	PART NUMBER	REV
1/1	C	0114-0340	B

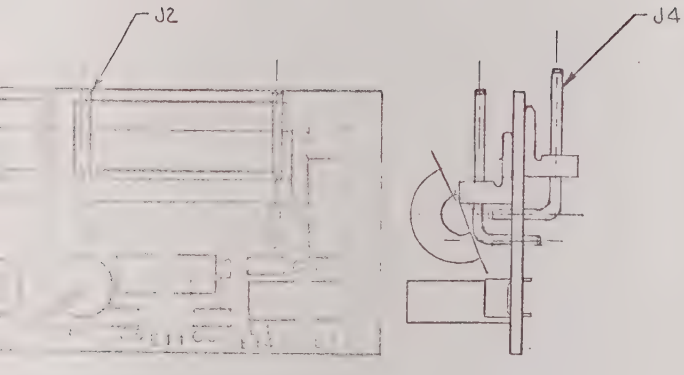
CODE | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED-

1. MARK LATEST REVISION LETTER WHERE SHOWN.
2. SCHEMATIC REF: 0114-0361.

REVISIONS						
ZONE	REV	ECO	DESCRIPTION	DWN	CHKD	DATE
	A	–	PROT			
	B	–	PILOT REL PER [illegible]			
	C	2320	[illegible]			
	D	2543	[illegible]			
	E	[illegible]	REVISED PER ECO	MAN	[illegible]	[illegible]



50 | 40 | 30 | 20 | 10	PART NUMBER	PART NAME				
DO NOT SCALE DRAWING	DRAWN	DATE	GOULD biomation			
	CHECKED		TITLE			
	PROJ. ENG.		FILTER BD. PWR. [illegible]			
	MANUFACTURING		SCALE	PART NUMBER	REV	
	QUALITY ASSUR.			D10114-0360	E	
				SHEET	OF	

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PART
	-60	-50	-40	-30	-20	-10	
1						1	0114
2							
3						1	1200
4							
5						2	3000
6						1	3000
7						5	3000
8						2	3000
9							
10						10	400
11						2	6000-
12						2	6000-
13						5	6400
14						5	6400
15							
16						5	9000
17							
18							

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
-10	0114-0[illegible]0	1	
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

RE

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	[illegible]				[illegible]
[illegible]	[illegible]	[illegible]		[illegible]	
[illegible]	RESISTOR	R3,4		[illegible] 1/4W 5%	
[illegible]	"	R5,11		10 Ω 1/4W 5%	
[illegible]	"	R6,10		2.7K 1/4W 5%	
[illegible]	"	R1,2		1.5K 1/4W 5%	
[illegible] 0025	CAP	C1-10		.1uf CERAMIC 50V 20%	
0410-08	CONNECTOR	J2,4		8PIN, RT ANG HDR	
0410-12	CONNECTOR	J1,J3		12PIN, RT ANG HDR	
[illegible]	LED	DS6-10		RED	
[illegible]	LED	DS1-5		GREEN	
[illegible]	INDUCTOR	L1-L5			LM

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PROTOTYPE	[illegible]	[illegible]		
	B	PROTOTYPE - REVISED	[illegible]	[illegible]	[illegible]	[illegible]
	C	REVISED PER ECO 2327		[illegible]	[illegible]	[illegible]
	D	REVISED PER ECO 2543	4-14-[illegible]	[illegible]	[illegible]	
	E	REVISED PER ECO 3585A	5-11-[illegible]	[illegible]	[illegible]	[illegible]

	DATE
[illegible]	[illegible]
[illegible]	[illegible]

LIST OF MATERIAL

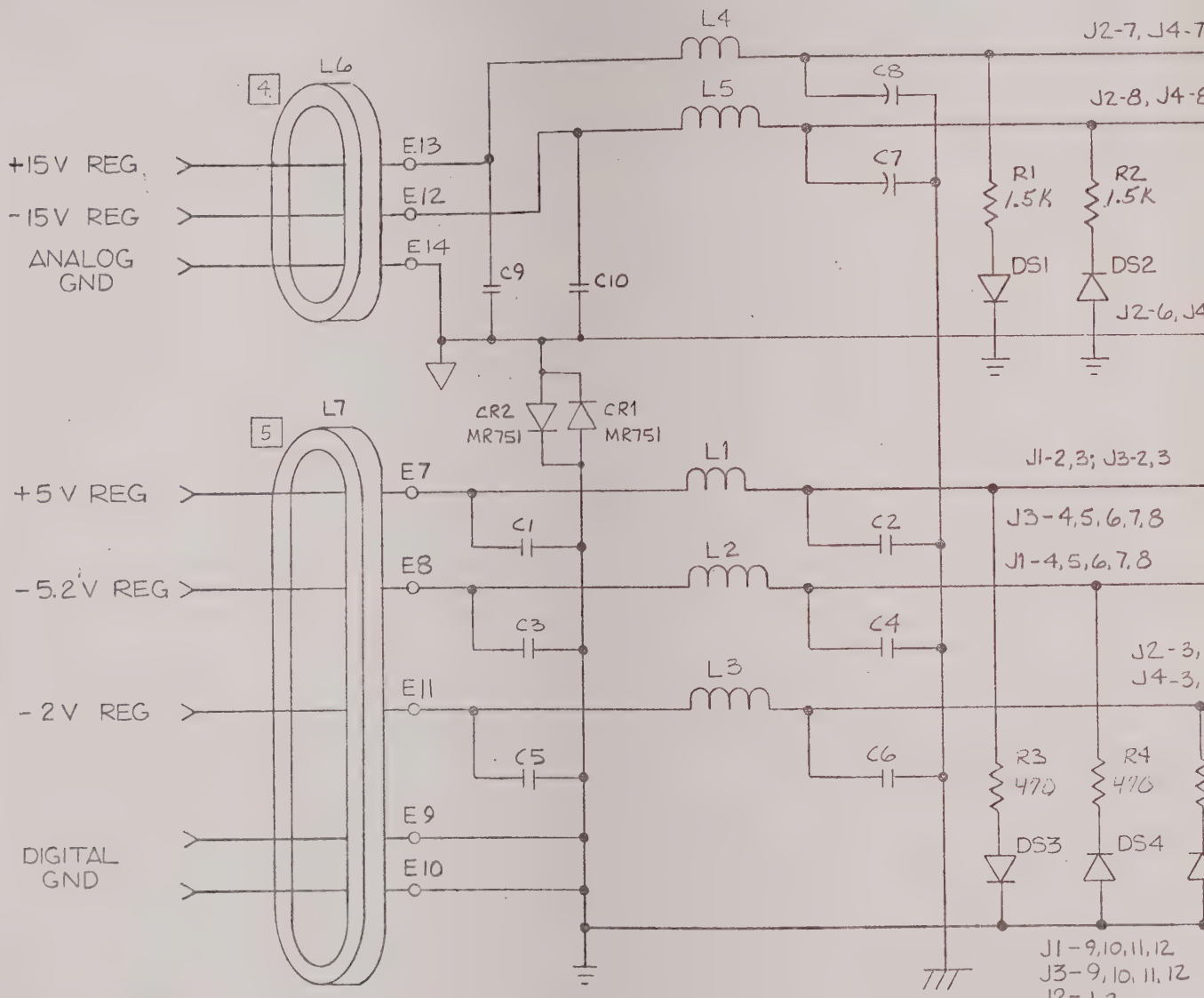
FILTER PW ASSY

POWER SUPPLY

biomation

B	0114-0360	REV E

MODEL K101-K5[illegible] | CODE | SHEET 1 OF 1



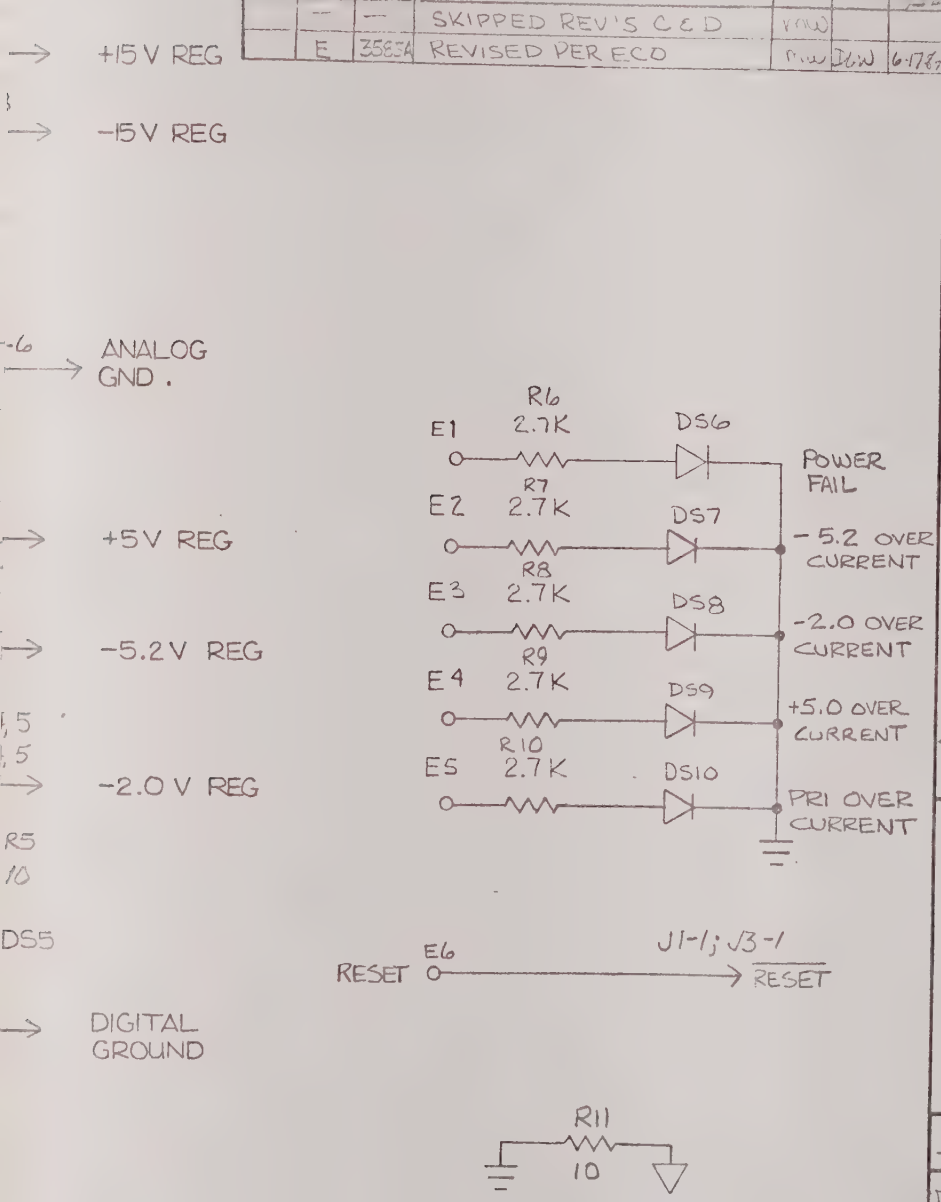
NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS; 1/4w; 5%.
2. ALL CAPACITORS ARE .1uf; 50V
3. LED'S DS1-5 ARE GREEN, DS6-10 ARE RED.
4. L6 IS ON ANALOG WIRE ASSY 0114-0367.
5. L7 IS ON DIGITAL WIRE ASSY 0114-0366.
6. ANALOG GROUND ▽ E14
7. DIGITAL GROUND ⏚ E9,10
8. CHASSIS GROUND ⏚

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

BISHOP GRAPHICS/ACCUPRESS REORDER NO A4428

REVISIONS						
ZONE	REV	FCO #	DESCRIPTION	DWN	CHKD	DATE
	A		PROTOTYPE	[illegible]		[illegible]
	B		PILOT REL PER ERN 0197	[illegible]	[illegible]	[illegible]
	B	[illegible]	REV'D PER ECO		[illegible]	[illegible]
	—	—	SKIPPED REV'S C & D	[illegible]		
	E	3583A	REVISED PER ECO	[illegible]	[illegible]	6-17-87



DWG. NO. 0114-0361 SH 1 REV. E

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010

HOLE SIZE: 0.599 ± .003; 600.999 ± .004; 1.000-1.499 ± .005

ENG SERV | DATE

DRAWN [illegible] | DATE 7-31-87

CHECKED [illegible]

PROJ. ENG.

MANUFACTURING

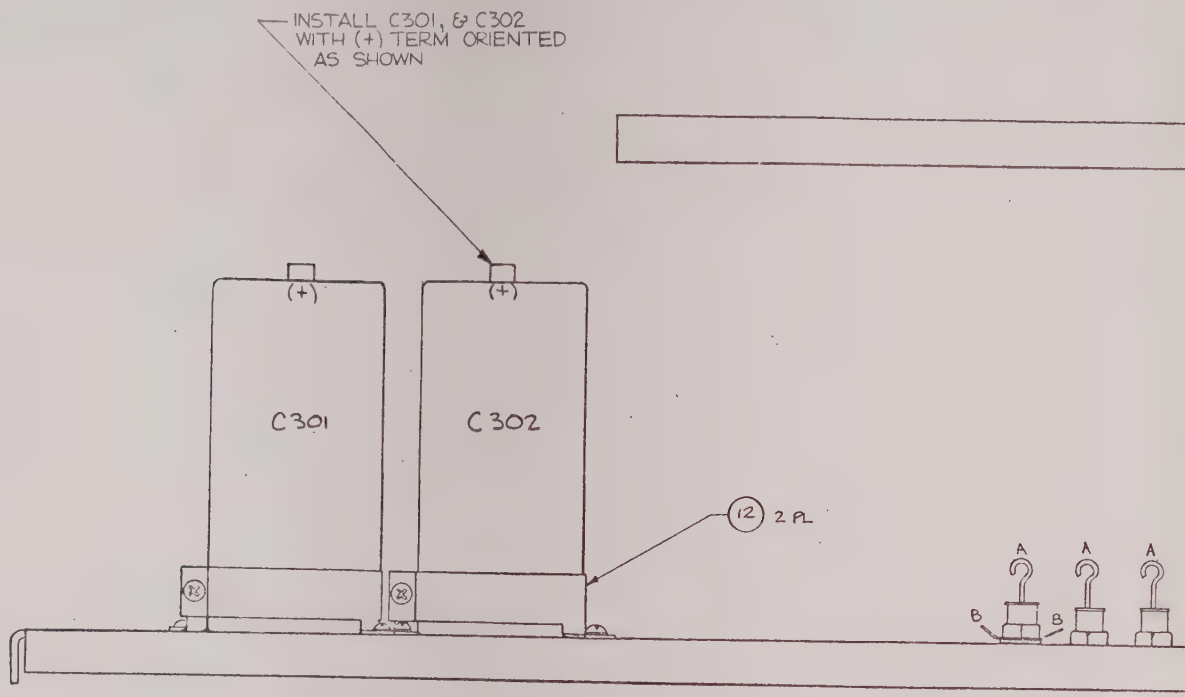
QUALITY ASSUR

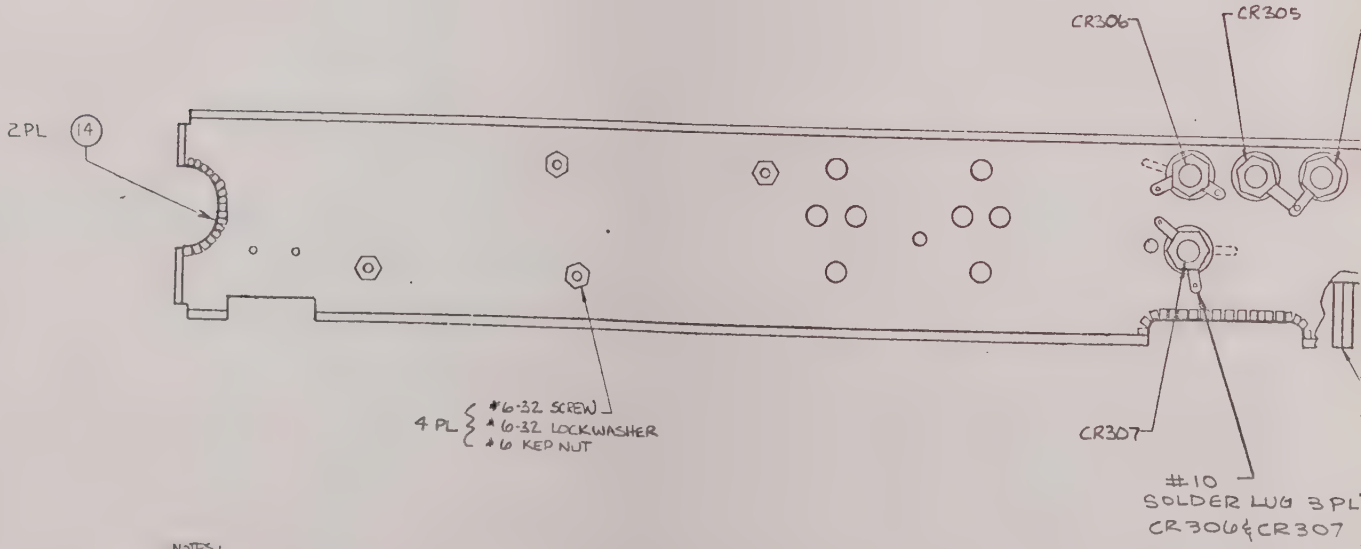
GOULD biomation

TITLE: FILTER BOARD SCHEMATIC

SCALE	SIZE	PART NUMBER	REV
—	C	0114-0361	E

CODE | SHEET 1 OF 1





NOTES:

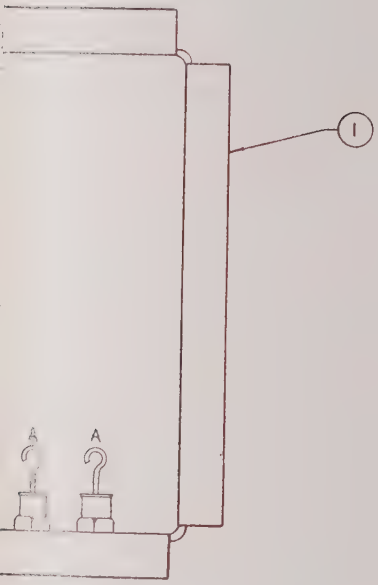
1. USE OF THERMAL COMPOUND REQ'D BETWEEN MICA WASHER AND HEATSINK.

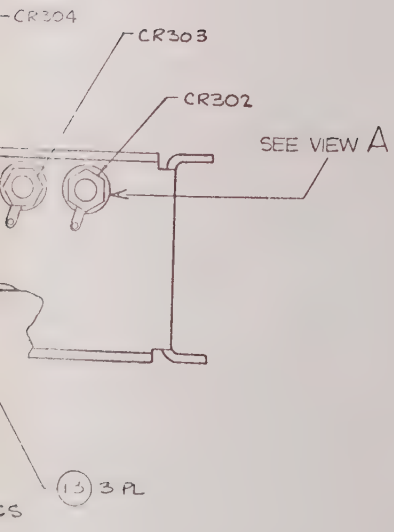
WIRE LIST

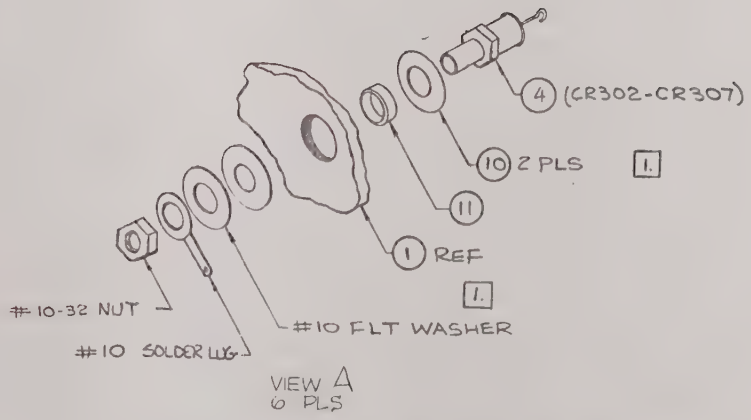
FROM	TO	AWG	DESCRI
CR307-B	CR305-A	16	ORG
CR306-B	CR304-A	16	BLK

DWG. NO. 0114-0330 SH 1 REV E

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	-	PROTOTYPE			
	B	-	PILOT REL PER ERN 0197			
	C	2236	REVISED PER ECO.	MS	RD	
	D	2630	" " "	DGW		
	E	2709	" " "	DGW		







DASH NO.	NUMBER	QTY
-10	0114-0320	1
	NEXT ASSEMBLY	

ITEM	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION
1			

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DRAWN 8 10 81

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: HEATSINK ASSEMBLY

SCALE	SIZE	PART NUMBER	REV
1/1	D	0114-0330	E

CODE | SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
1						1	011-
2							
3							
4						6	120
5							
6							
7							
8						2	440
9							
10						12	700
11						6	700
12						2	700
13						3	700
14						A/R	720
15							
16						A/R	7150
17						A/R	7150
18							

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURIN
			QUALITY ASSU
-10	011-0330		
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0326	HEATSINK				FAB
-0293	RECTIFIER	CR302-307		IN6096	
-0046	CAP	C301, C302		2000uf 200V	
-0442	MICA WASHER			#10	
-0441	SHOULDER WASH			.280 O.D. X .200 I.D.	
-0164	BRACKET	@ C301, C302			
-0421	STANDOFF, HEX			6-32 x 3/4	
-0044	FLEXIBLE GROMMET				
-0016-10	WIRE			16 AWG BLK	
-0016-03	WIRE			16 AWG ORG	

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	6-24-81	[illegible]		
B	PILOT REL PER ERN 0197	9/21/81	[illegible]	[illegible]	
C	REVISED PER ECO #2236	10/14/81	[illegible]	[illegible]	
D	" " " #2230	[illegible]	[illegible]		
E	" " " #2709	[illegible]	[illegible]		

	DATE
	6-29-81
[illegible]	10-15-81

LIST OF MATERIAL

HEAT SINK ASSY

biomation

B | 0114-0330 | REV E

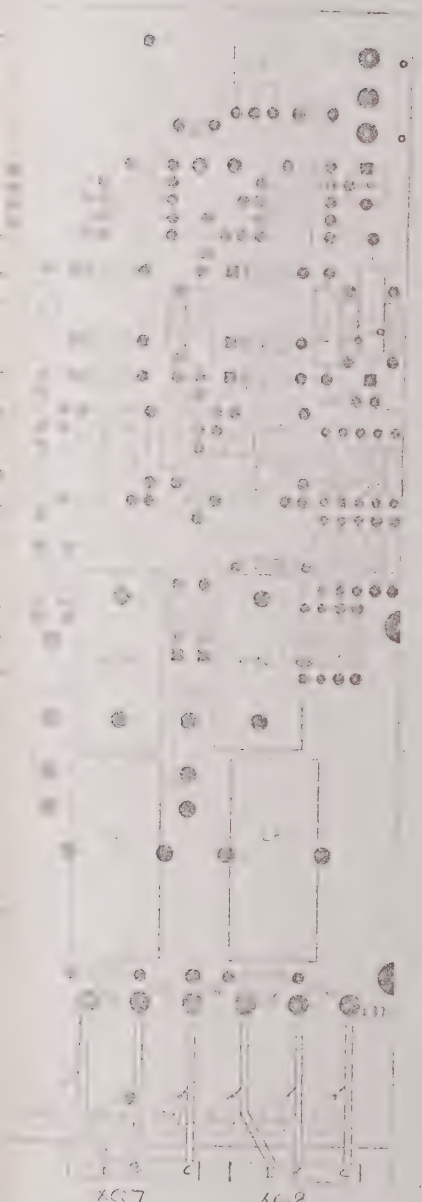
MODEL K101/K500 | CODE | SHEET 1 OF 1

NOTE

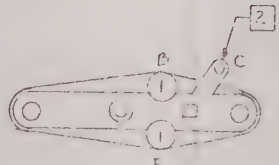
1. R41, 51, 53, 54, 95, 96, 125, 63, 64 ARE TO BE MOUNTED ON THE FAR SIDE OF THE P.C.B.
2. DRILL OUT "C" HOLE (.125 DIA) ON XQ18 & XQ20.
3. SEE TOP ASSY 0285-0003.
4. (C23 & C73 TO BE MOUNTED ON THE SOLDER SIDE OF PCB)

LEFT SIDE

Q	—	
R	1781	REVISED PER ECO
S	1785	REVISED PER ECO
T	1831	REVISED PER ECO
U	1852	REVISED PER ECO
V	1859	REVISED PER ECO
W	1980	REVISED PER ECO
X	2018	REVISED PER ECO
Y	2043	REVISED PER ECO
Z	2152	REVISED PER ECO
AA	2291	REVISED PER ECO
BB	2420	REVISED PER ECO
CC	2433	REVISED PER ECO
DD	2508	REVISED PER ECO
EE	2629	REVISED PER ECO
FF	2639	REVISED PER ECO
GG	2722	REVISED PER ECO
HH	2733	REVISED PER ECO
JJ	3516	REVISED PER ECO *
KK	3614	REVISED PER ECO *



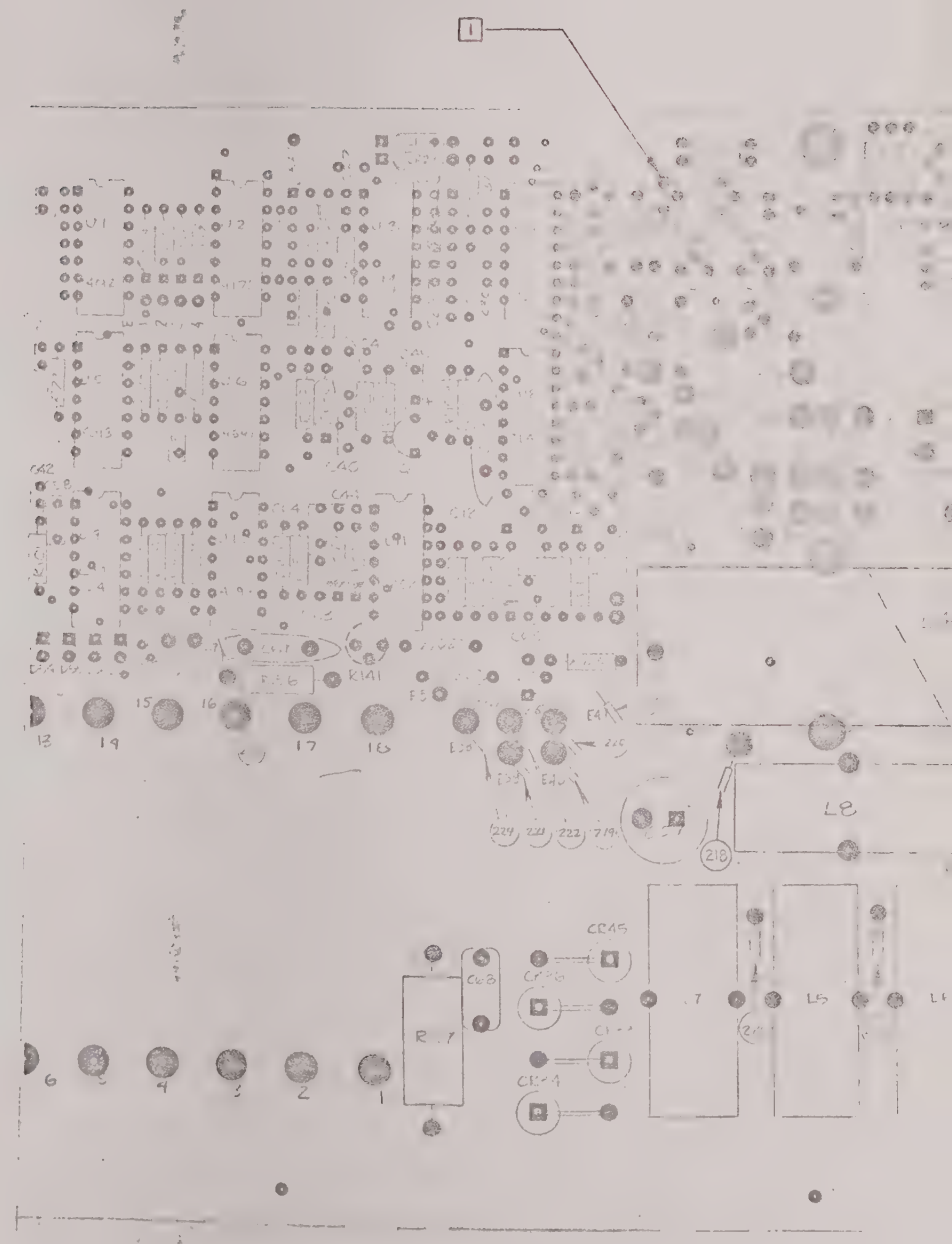
SEE DETAIL A



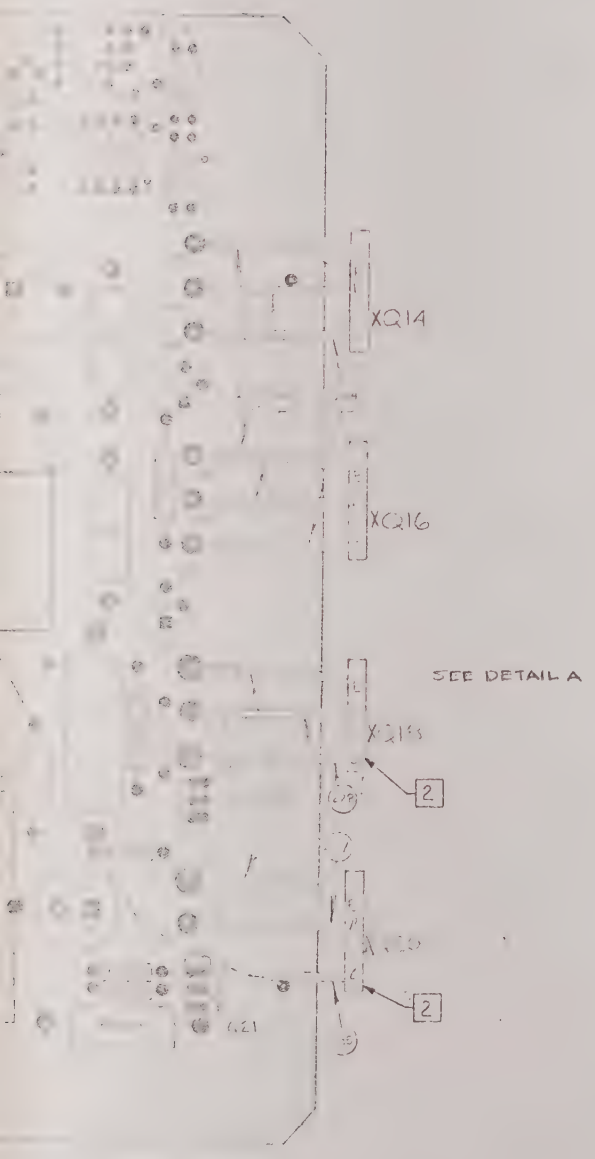
DETAIL A

REAR VIEW

GOULD biomation



RIGHT SIDE


XQ14
XQ16
SEE DETAIL A
2
2

WIRE LIST				
WIRE No	FROM	TO	ITEM No	DESCRIPTION
1				[3]
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16	E16		[illegible]	BRN
17	E17		208	RED
18	E18	P3	216	TAN
19	E19	P4	216	TAN
20	E20		215	BLK
21	E21		214	VIO
22	E22		213	YEL
23	E23		212	CKG
24	E[illegible]		N/C	—
25	E[illegible]		[1]	[1]
26	E[illegible]		227	GRN/YEL
27	E27		[1]	[1]
28	E28		211	RED
29	E29		210	BRN
30	E30		211	RED
31	E31		210	BRN
32	E32	XQ7 E	201	RED
33	E33	XQ7 B	209	BLK
34	E34	XQ7 C	207	BLK
35	E35	X[illegible]	[illegible]	RED
36	E36	X[illegible]	205	BRN
37	E37	XQ8 C	207	BLK
38				
39	E39		221	[illegible]
40	E40		222	[illegible]
41	E41		211	RED
42	E42		220	RED
43				
44	E44		[illegible]	BRN
45	E45		223	YEL
46	E46		220	WHT/RED
47	E47	XQ14 E	201	RED
48	E48	XQ14 B	200	BRN
49	E49	XQ14 C	209	BLK
50	E50	X[illegible] E	201	RED
51	E51	X[illegible]	[illegible]	BRN
52	E52	X[illegible]	209	BLK
53	E53	XQ15 [illegible]	234	RED
54	E54	X[illegible]	209	BLK
55	E55	XQ1[illegible]	[illegible]	BLK
56	E56	X[illegible]	234	RED
57	E57	X[illegible] B	204	BLK
58	E58	X[illegible] C	235	BLK
59	E59	P1	216	BLK
60	E60	P2	[illegible]	BLK
61	E61	—	180	BRN
62	E62	—	181	RED
63	E70	—	214	VIO
64	T16	E71	—	WHT (IF USED)

4 3 1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

D C B A

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE

SIZE D | PART NUMBER | REV

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	-10	
1					1		
2							
3					15		
4							
5					10		
6							
7							
8					1		
9							
10					3		
11							
12					1		
13					2		
14							
15					1		
16					4		
17							
18							

ASSEMBLY TIME	COMPONENT LEAD SPACING

			DRAWN
			CHECKED
			ENGINEER
			MANUFAC
			QUALITY
DASH NO.	NUMBER	TITLE	
	NEXT ASSEMBLY		

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
5-0012	PWB				FAB
	DIODE	CR1-2, 24-26, 28,	37-39	1N4152	
-0031	DIODE	CR10, 11, 16, 17,	19-23, 28	1N4937	
0-0026	DIODE BRIDGE	CR1		VE18X	
0-0014	DIODE	CR14, 15, 46		1N4004	
0-0015	DIODE	CR 31		1N825	
0-0043	DIODE	CR4, 5		1.5KE220	
-0022	DIODE	VR1		1N5245	
-0035	DIODE	CR33, 34, 36, 45		MR850	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	[illegible]				
	B	[illegible]				
	C	[illegible]				
	D	CHANGED PER ECO # 1486				
	E	UPDATED PER PILOT RUN ECO 1521				
	F	ECO 1554				
	G	ECO 1568				

DATE

LIST OF MATERIAL

POWER SUPPLY

ASSY - PWA

biomation

B | 0205-0010 | REV

[illegible]

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY						
	QD		AD				
19							
20							
21					1		
22					5		
23					1		
24					1		
25					1		
26							
27					1		
28							
29							
30							
31							
32					1		
33							
34					1		
35					1		
36					1		

SSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M B

CHECKED

ENGINEER

MANUFACTURIN

QUALITY ASSUR

T NUMBER	PART NAME	[illegible] DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	TRANSISTOR	[illegible]		2N2219	
[illegible]		[illegible]		2N[illegible]	
[illegible]		Q21		2N6131	
[illegible]		Q15		2N2905	
D-0026	TRANSISTOR	Q19		2N6134	
D-0019	TRANSISTOR	Q11		2N3906	
[illegible]	TRANSISTOR	Q4		2N3439	
D-0047	I.C.	Q1		LM340T	
D-0078	RES PACK	RP1		100K	
D-0077	RES PACK	RP2		4.7K	

EF. DRAWINGS	REV	DESCRIPTION	DATE	D[illegible]	CKD	APP'D
	H	ECO 1621	[illegible]	[illegible]	[illegible]	
	J	ECO 1686	[illegible]	[illegible]	[illegible]	
	K	ECO 1680	[illegible]	[illegible]	[illegible]	
	L	ECO 1689	[illegible]	[illegible]	[illegible]	
	M	ECO 1683	[illegible]	[illegible]	[illegible]	
	N	ECO 1697	[illegible]	[illegible]	[illegible]	
	P	ECO 1728	[illegible]	[illegible]	[illegible]	

RTDN)	DATE 11-20-80
ANCE	

LIST OF MATERIAL

POWER SUPPLY
ASSY PWA

biomation

B	0235-0010	REV KK
CODE		SHEET 2 OF /

MODEL [illegible]

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	10	CAT
37							
38							
39							
40					1		1700
41					3		1700
42							
43					1		1826
44					1		
45					1		
46					1		
47					1		
48					1		
49					1		13
50							
51					1		17
52							
53							
54							

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	
CHECKED	
ENGINEER	
MANUFACTURIN	
QUALITY ASSUR	

PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
I.C.	U12		LM358	
I.C.	U3,4,9		LM324	
CMOS	U6		14541	
	U2		14175	
	U11		14002	
	U1		14012	
	U5		14013	
	U10		14093	
TRANSISTOR	U14		4N35	
I.C.	U8		TL494	

WINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	Q	ECO 1736	5-14-8	KH	[illegible]	
	R	PRODUCTION RELEASE PER ECO #0152	[illegible]	[illegible]	RG	
	S	REVISED PER ECO #1781	[illegible]	[illegible]	[illegible]	
	T	REVISED; ECO #1785	6-10-8	[illegible]	[illegible]	
	U	REVISED; ECO #1831	8-24-8	MK	[illegible]	
	V	REVISED; ECO #1859	[illegible]	[illegible]	[illegible]	

DATE [illegible]

LIST OF MATERIAL

POWER SUPPLY

ASSY PWA

biomation

B | 0285-0010 | REV KK

MODEL 4500 | CODE | SHEET 3 OF 11

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -20	-50	-40	-30	-20	-10	PA
55							
56					2		3
57					2		3
58					12		
59							
60					6		
61					1		
62							
63					3		
64							
65					1		
66					8		
67					2		
68					1		
69					1		
70					1		
71							
72					1		3

			DRAWN M Ba
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	RESISTOR	R100, 121		150K 1/4W 5%	
	RESISTOR	R87, 90		100Ω 1/4W 5%	
		R45, 70, 77, 86, 88,		10K	
		93, 106-108, 110, 125, 144			
		R1, 78, 84, 103, 104, 136		100K	
		R142		22K	
		R105, 154, 153		2.2MEG	
		R97		4.3K	
		R23, 24, 51, 101, 117-119, 152		2.2K	
		R135, 137		220Ω	
		R13		1.5K	
		R50		180Ω	
		R102		180K	
	RES	R121		1.1K, 1W, 5%	

DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APP'D
	W	REVISED; ECO#1980				
	X	REVISED PER ECO #2018				
	Y	REVISED PER ECO #2083				
	Z	REVISED PER ECO. #2152				
	AA	REVISED PER ECO #2199				
	BB	REVISED PER ECO # 2420				

DATE 11-20-80

LIST OF MATERIAL

POWER SUPPLY

ASSY PWA

biomation

B | 0285-0010 | REV

MODEL 4500 | CODE | SHEET 1 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	
73					1		310
74					1		300
75							
76					5		
77					2		300
78					1		300
79					1		300
80					1		300
81					4		
82							
83					3		
84					3		
85					3		
86					3		300
87							
88					2		300
89							
90					1		300

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN

CHECKED

ENGINEER

MANUFACTURIN

QUALITY ASSUR

PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYP
[illegible]-262	RESISTOR	R85		19.6K 1/2W 1%	
[illegible]	RESISTOR	R12		470K [illegible]	
[illegible]-[illegible]04		R42-44, 47, 45		6.8Meg	
0-5103		R55, 57		510K,	
[illegible]-2401	RES	R 140		2.4K, 1/4W, 5%	
0-2702	RES	R145		27K, 1/4W, 5%	
[illegible]-[illegible]700	RESISTOR	R14		470Ω 1/4W 5%	
-4706		R27, 28, 126 (R115-20 ONLY)		47Ω	
-4701		R18, 21, 22,		4.7K	
-5601		R15, 80, 112		5.6K	
-5101		R45, 46, 146		5.1K	
[illegible]-[illegible]1	RESISTOR	R19, 20, 109,		2.7K 1/4W 5%	
[illegible]-[illegible]206	RESISTOR	R31, 32		82Ω 1/4W 5%	
[illegible]	RESISTOR	R17		[illegible]	

REV	DESCRIPTION	DATE	DWN	CKD	APPD
[illegible]	REVISED PER ECO # 2508	[illegible]	[illegible]	T.J.	
[illegible]	REVISED PER ECO# 2629	11-17[illegible]	[illegible]	[illegible]	
FF	REVISED PER ECO# 2632	11-178[illegible]	[illegible]	DGW	
[illegible]	REVISED PER ECO# 2722	[illegible]	[illegible]	[illegible]	
HH	REVISED PER ECO# 2733	[illegible]	[illegible]	[illegible]	
JJ	REVISED PER ECO #3516	[illegible]	[illegible]	—	—
KK	REVISED PER ECO# 3600A	[illegible]	MW	DGW	[illegible]

DATE 11 20 [illegible]

LIST OF MATERIAL

POWER SUPPLY

ASSY PWA

biomation

B 0235-0010 REV KK

MODEL 4500 CODE SHEET [illegible] OF [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PAR
91							
92					1		3
93					1		
94					4		
95					2		
96					1		
97					1		
98					2		3000
99					2		3100
100					1		300
101							
102					1		3000
103							
104							
105					1		3100
106					1		3102
107					1		3100
108							
							RE

			DRAWN M G
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURA
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
			47K 1/4W 5%	
			4.7K	
	R66,67,138 (R116-20 ONLY)		1K	
	R59, 62		13K	
	R60		33K	
	R79		11K	
	R41, 82		20K 1/4W 5%	
	R83, 122		20K 1/8W, 1%	
RESISTOR	R52		8.2K 1/4W 5%	
RESISTOR	R49		15K 1/4W 5%	
	R123		150K 1/8W, 1%	
	R127		5.62K	
RESISTOR	R128		3.92K 1/8W 1%	

F. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DATE 11-20-

LIST OF MATERIAL

POWER SUPPLY

ASSY PWA

biomation

B | 0285-0010 | REV K

MODEL 4500 | CODE | SHEET 6 OF

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
110							
111					8		312
112							
113					1		310
114					1		310
115					2		305
116					2		
117							
118					1		320
119							
120					2		307
121					1		307
122					1		305
123					2		0235
124							
125					2		308
126					1		308
127					1		307

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	M.L.
CHECKED	
ENGINEER	
MANUFACTURIN	
QUALITY ASSUR	

RT NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-1002	RESISTOR	R56, 58, 68, 69, 73, 74		10K 1/4W .5%	
		71, 72			
3871	RESISTOR	R158		8.87K, 1/8W, 1%	
1151	RESISTOR	R159		1.15K, 1/8W, 1%	
-1507	RESISTOR	R25, 26		1.5Ω 1/2W 5%	
-5200		R29, 30		820Ω 1/2W 5%	
0-0039	RESISTOR	R139		22Ω, 2W	
0-3000	RESISTOR	R100, 131		300Ω 1W 5%	
0-4700	RESISTOR	R3		470Ω 1W 5%	
0-1007	RESISTOR	R143		1Ω, 1/2W, 5%	
[illegible]	RESISTOR	R90, 91		1.2MILLIOHM	
0-5002	RESISTOR	R10, 11		56K 2W 5%	
0-3106	RESISTOR	R157		51Ω 2W 5%	
0-1206	RESISTOR	R156		12Ω 1/2W 5%	

WINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE

LIST OF MATERIAL

POWER SUPPLY

[illegible] PWA

biomation

B [illegible]

MODEL 4500

CODE

SHEET [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PAR
	-60	-50	-40	-30	-20	-10	
128							
129					1		3200
130					3		320
131					2		320
132					1		3
133							
134					2		0
135					1		0230
136					2		3
137							
138					5		330
139					5		3
140							
141							
142							
143							
144							
145							

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
0-0037	RESISTOR	R16		3.0K 5W	
[illegible]3	RESISTOR	R33,34,133		10Ω 5W	
[illegible]-0035	RESISTOR	R35,36		500Ω 10W	
[illegible]06	RESISTOR	R99		39Ω 2W 5%	
[illegible]-0199	RESISTOR COIL	R75,76		10 Milli Ohm	
-0[illegible]-10	RESISTOR COIL	R89		2 Milli Ohm	
[illegible]	RESISTOR	R132,134		47Ω 3W 5%	
0-0005	VAR. RESISTOR	R53,54,94-96		200Ω	
[illegible]	VAR. RESISTOR	R[illegible],64,[illegible],12[illegible],141		5K	

[illegible]NGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE	LIST OF MATERIAL	bicmation
		[illegible] SUPPLY [illegible] PUMP	B 0255-0010
		MODEL [illegible]	CODE SHEET [illegible]

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	-10	PAR
146							
147					1		401
148					1		401
149					3		400
150					20		400
152					9		400
153					2		4:0
154					1		4:0
155					1		4050
156					3		410
157					3		410
158					2		401
159							
160					1		430
161					2		401
162							
163							

ASSEMBLY TIME

COMPONENT LEAD SPACING

DRAWN BY

CHECKED

ENGINEER

MANUFACTURING

QUALITY ASSU

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0101	CAPACITOR	C60		100 PF	
[illegible]	CAPACITOR	C14,		.01uf 50V	
[illegible]49		C6, 7, 67		.01uf 1KV, 20%	
[illegible]04		C1,8,19,20,27-32,	43,	.1uf, 50V	
		50,57,61,63-66	(C25,62,-20 ONLY)		
[illegible]	CAPACITOR	[illegible],37, 33, 34, 42,	44, 47, 49,59	.01uf, 100V	
[illegible]7	CAPACITOR	C22, 23		.01uf, 400V POLYPROPOLENE	
[illegible]	CAPACITOR	C39		.01uf, 100V	
-0007	CAPACITOR	C58		1uf, 50V	
-0015	CAPACITOR	C15, 16, 36		1000 pf, 500V	
-0018	CAPACITOR	C17, 18, 35		330 pf, 500V	
-0471	CAPACITOR	C70, 41		470pf 50V/100V	
[illegible]	CAPACITOR	C45		4.7uf, 50V	
-0822	CAPACITOR	C40, 69		.0082uf, 50V, 10%	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE 11 20 [illegible]	LIST OF MATERIAL POWER SUPPLY ASSY PWA	biomation
			B [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
164					1		44
165					1		41
166					3		47
167					2		47
168					1		43
169							
170							
171					1		43
172					1		40
173					2		42
174					1		4
175							
176							
177					4		64
178							
179							
180					1		02
181					1		02

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN

CHECKED

ENGINEER

MAINTENANCE

QUALITY ASSURANCE

RT NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	CAPACITOR	C2		470uf 25V	
[illegible]	CAPACITOR	C48,		390 uf, 50V	
[illegible]50	CAPACITOR	C53,54,55		470uf, 12V	
[illegible]052		C51,52		470uf/50V	
[illegible]009		C21		22uf, 15V	
[illegible]-0036		C11		6uf, 200V	
[illegible]-0050	CAPACITOR	C43		.005 uf	
[illegible]041	CAPACITOR	C4,5		47uf, 400V	
[illegible]051	CAPACITOR	C3		2200 uf, 25V	
[illegible]-0039	L.E.D.	DS4,5,6,7		RED	
[illegible]-0221-10	WIRE ASSY				
[illegible]-0221-20	WIRE ASSY				

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE 11 20 80

LIST OF MATERIAL

POWER SUPPLY ASSY [illegible]

biomation

B | 0285-0010 | REV K[illegible]

MODEL [illegible] | SHEET [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	P
182					1		5.1
183							
184							
185							
186					1		25
187					1		90
188					2		90
189							
190					1		90
191					1		90
192					2		90
193					1		90
194					2		90
195					1		90
196					2		90
197							
198							
199					1		

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN

CHECKED

ENGINEER

MANUFACTUR

QUALITY ASS

PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	NEON LAMP	DS3	NE2		
[illegible]	TRANSFORMER	T1		LINE XFMR 115/[illegible]	
[illegible]164	TRANSFORMER	T2,		INPUT BALUN XFMR 2213	
[illegible]0075	TRANSFORMER	T4, T5		BASE DRIVE XFMR	
[illegible]	TRANSFORMER	T7		CURRENT [illegible] XFMR	
[illegible]	INDUCTOR	L6		12μh	
[illegible]	INDUCTOR	L2, L3		[illegible]	
[illegible]-0079-10	INDUCTOR	L5		HI-CURRENT OUTPUT INDUCTOR, 45 uH	
[illegible]	INDUCTOR	L7, L8		LO-[illegible]	
[illegible]0083	INDUCTOR	L4			
[illegible]	INDUCTOR	L9, L10			

REVISIONS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE
[illegible]	[illegible]
[illegible]G	
[illegible]RANCE	

LIST OF MATERIAL

POWER SUPPLY

ASSY PWA

biomation

B	0295-0010	[illegible]

MODEL [illegible]

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	10	
200					2		
201					3		
202					—		
203					—		
204					5		
205					1		
206					1		
207					1		
208					1		
209							
210					2		
211					2		
212					1		C4-5
213					1		
214					1		
215					1		
216					1		C2-3
217					—		

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

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ENGINEER
MANUFACTURIN
QUALITY ASSUR

RT NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]-10	WIRE FAB			BRN	
-20				RED	
-30				BLK	
-40				RED	
-50				BLK	
-60				BRN	
-70				RED	
-80				BLK	
[illegible]	CABLE ASSY			RED BRN	LM
[illegible]-10	"			BRN	LM
-20	"			RED	LM
[illegible]-10	ASSY, [illegible]			[illegible]	LM
[illegible]	"			YEL	LM
-10	"			[illegible]	LM
[illegible]	"			BLK	LM
[illegible]-10	CABLE ASSY, FAN			BLK, TAN	LM
[illegible] 91	CABLE FAB			BLK	

EF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE
	[illegible]

LIST OF MATERIAL

POWER SUPPLY

biomation

B

MODEL 4500 | CODE | SHEET 2 OF [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10
219					1	
219					1	
220					1	
221					1	
222					1	
223					1	
224						
225						
226					1	
227					1	
228					—	
229					2	
230					4	
231						
232					2	
233					1	
234					2	
235					1	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN
CHECKED
ENGINEER
MANUFACTUR
QUALITY ASS

ART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]-01	RECT WIRE FAB			RED	
-03				BLU	
-04				WHT	
-05				ORG	
-06				GRY	
-07				YEL	
-10				WHT/BLK	
[illegible]	WIRE FAB			GRN/YEL	
[illegible]	WIRE FAB			BLK	
[illegible]	SOCKET	X C18, 20		.050 DIA TERM.	
[illegible]	"	X C7, 8, 14, 16		.040 DIA TERM.	
00-0029	MOUSE TAIL			3" LONG	
[illegible]	CABLE ASSY			BLACK	
[illegible]	CABLE ASSY			RED	
[illegible]	CABLE ASSY			BLUE	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

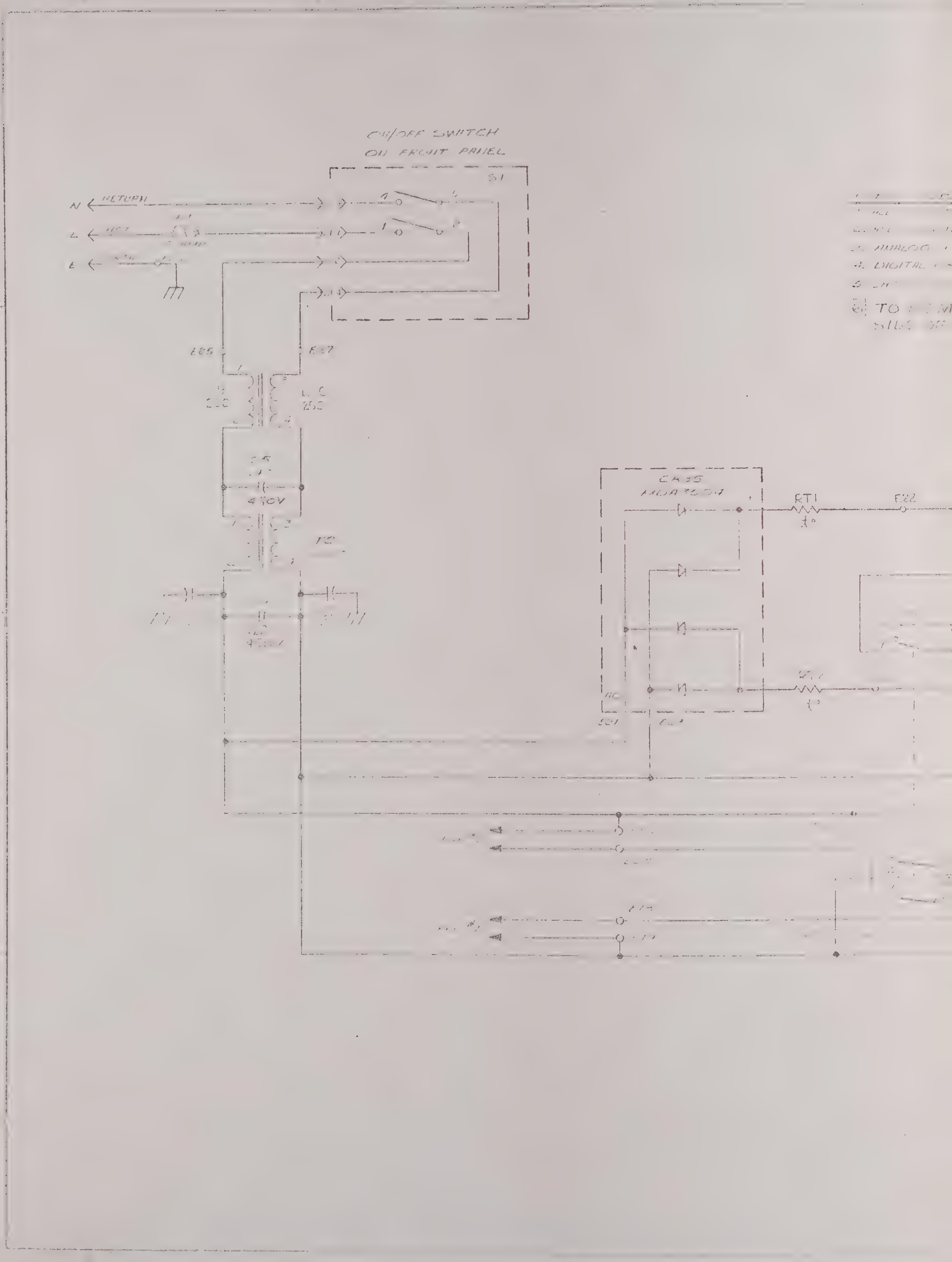
LIST OF MATERIAL

POWER SUPPLY

biomation

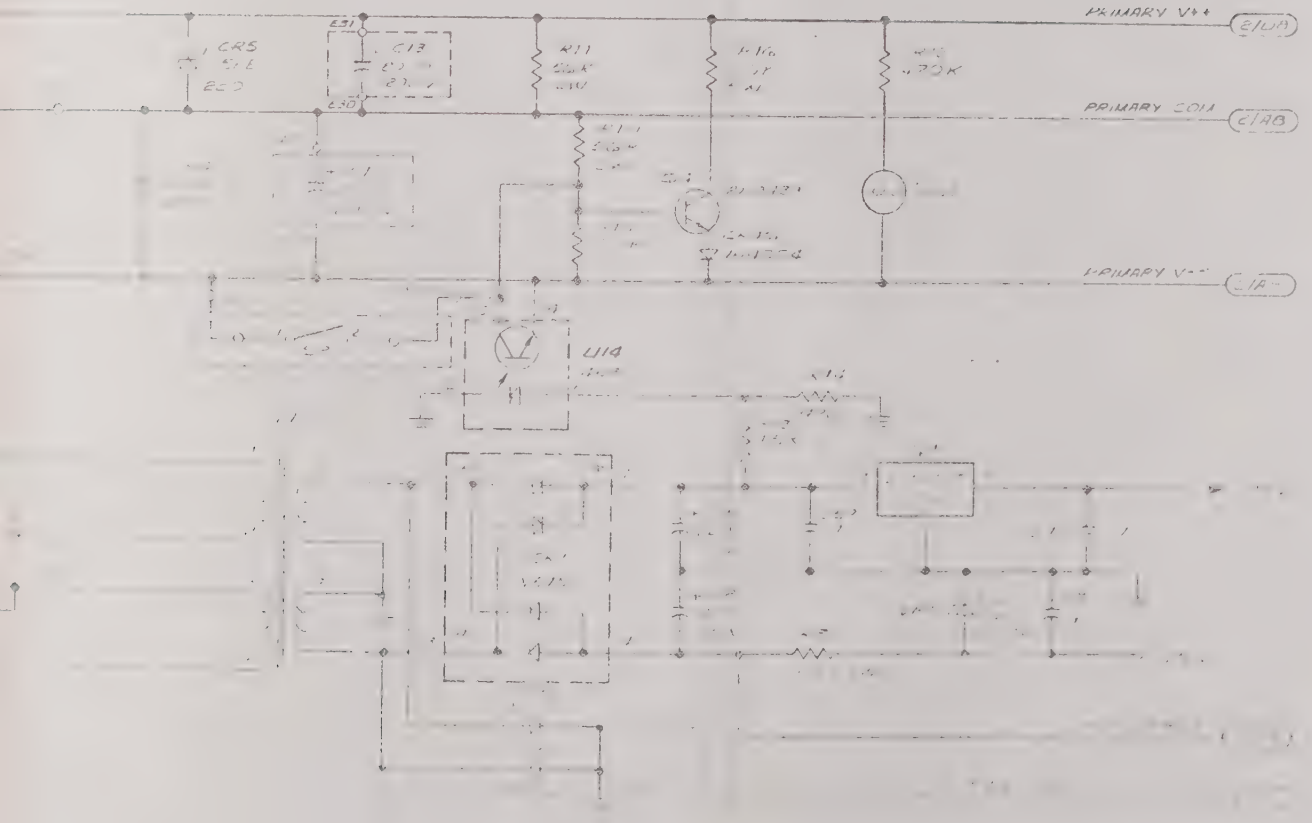
B | 0235-0010

MODEL 4500


ON/OFF SWITCH
ON FRONT PANEL
S1
N
RETURN
L
E
410V
RT1
E22
ANALOG
DIGITAL
TO

UNLESS SPECIFIED
RESISTOR VALUES ARE IN OHMS, ¼ W, 5%
CAPACITOR VALUES ARE IN MICRO FARADS
GROUND V
GROUND ⏚
GROUND (1)

MOUNTED ON SOLDER BOARD



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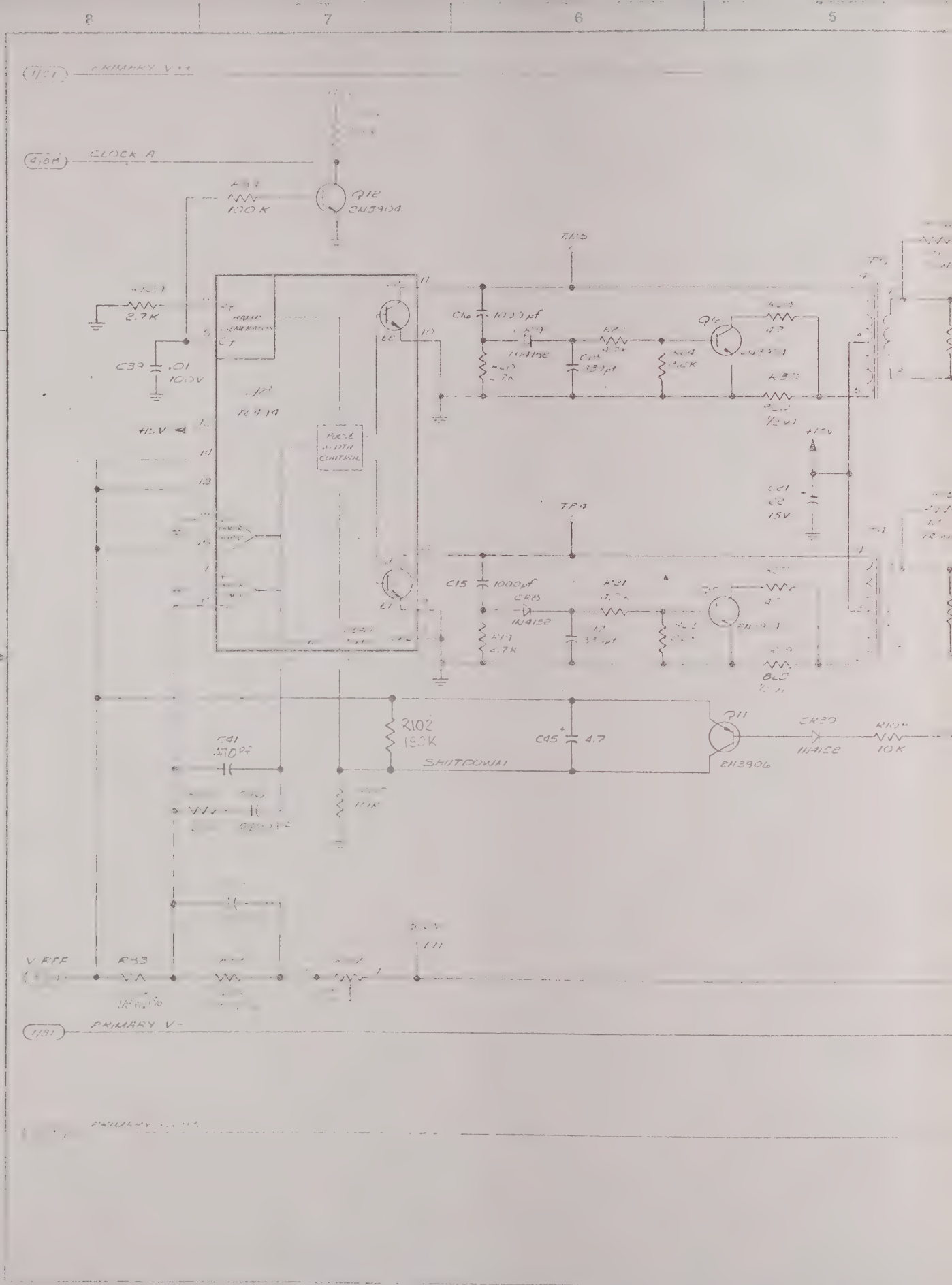
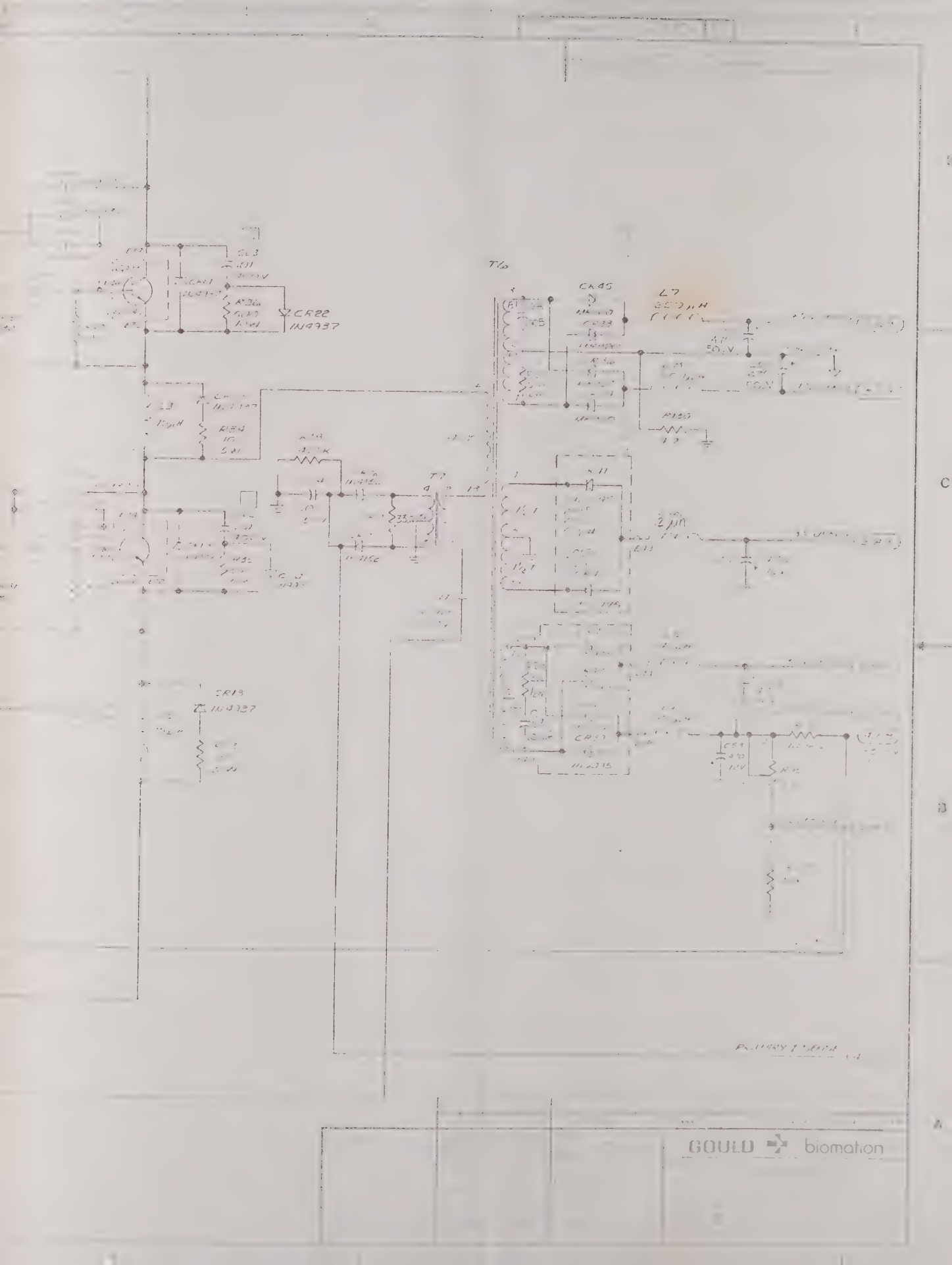
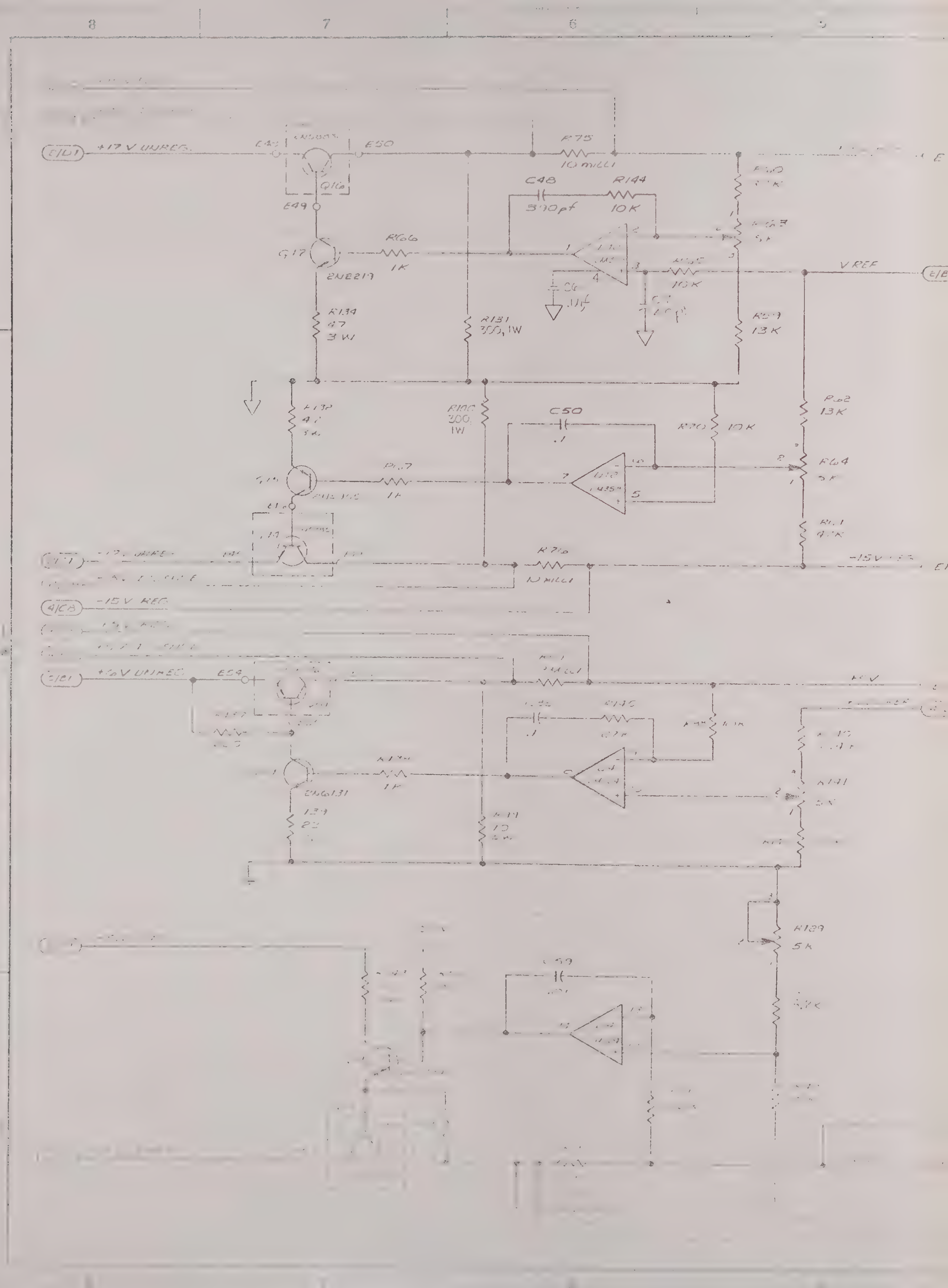
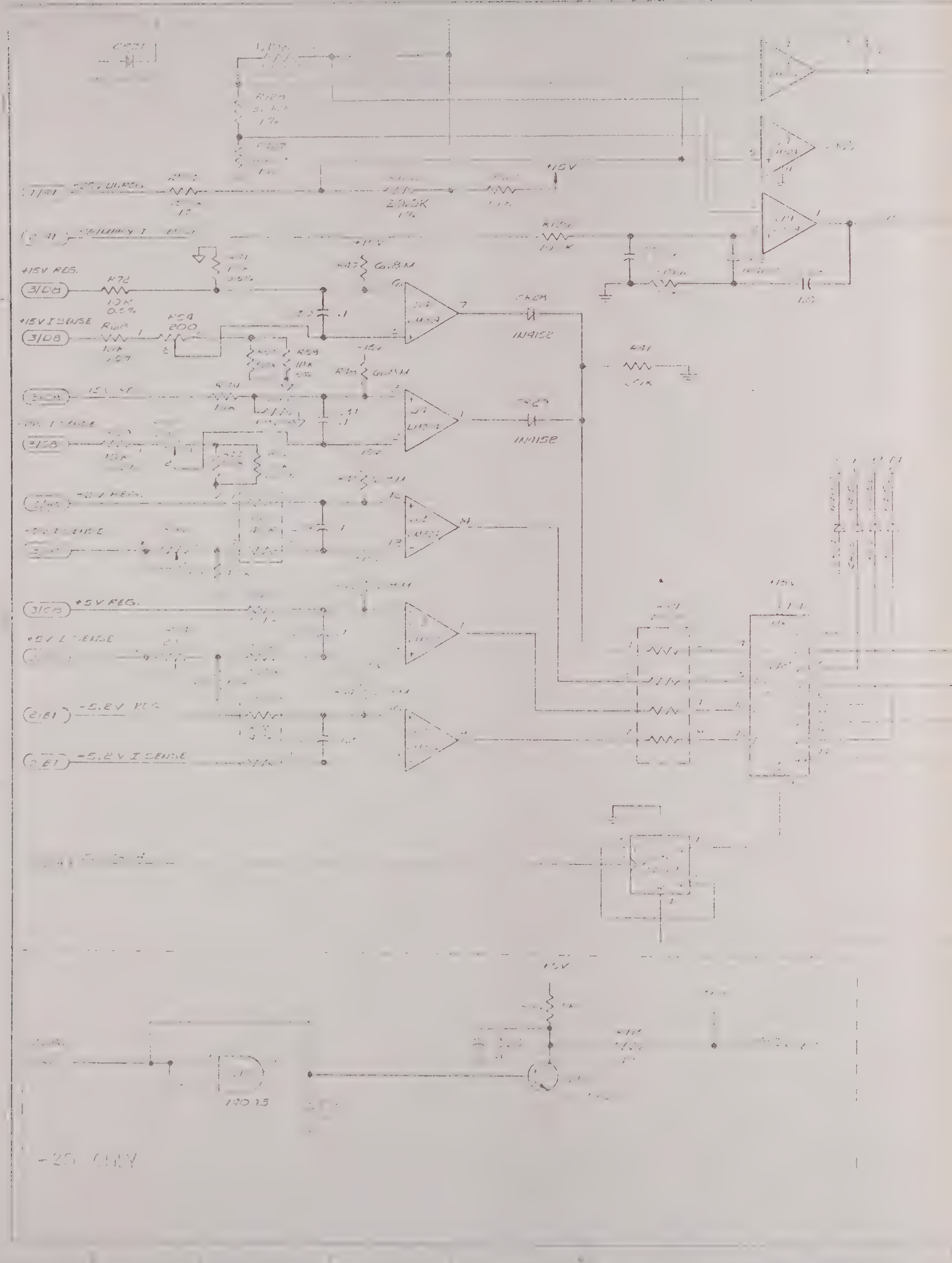


8
7
6
5
PRIMARY V++
CLOCK A
Q12
2N3904
100 K
2.7K
C39
.01
100V
+15V
PULSE WIDTH CONTROL
TP5
C16
1000pf
Q6
TP4
C15
1000pf
CR8
1N4152
R17
2.7K
R102
180K
C45
4.7
SHUTDOWN
Q11
2N3906
CR30
1N4152
R104
10K
C41
470pf
V REF
R33
PRIMARY V-

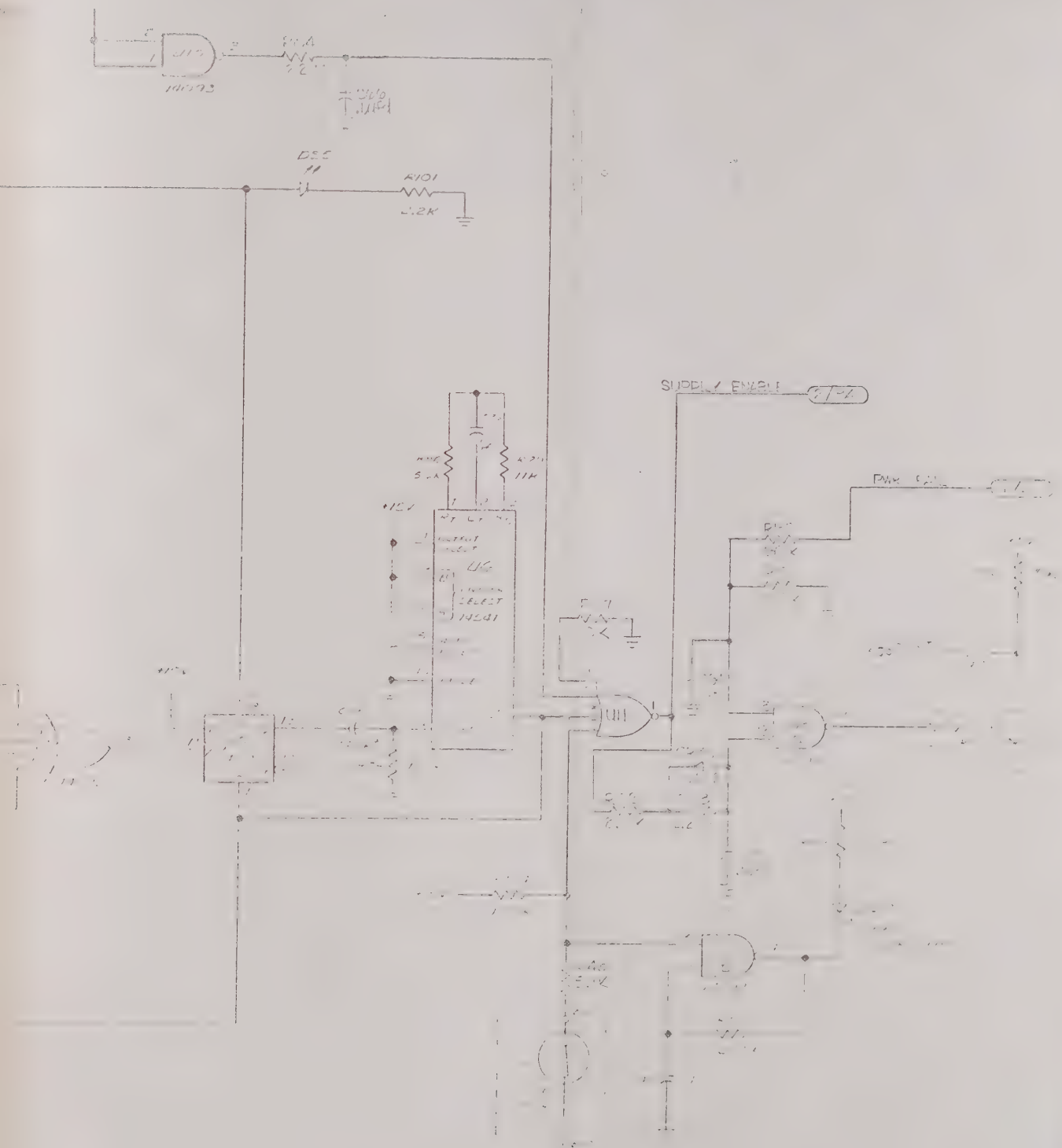

CR22
1N4937
CR45
L7
CR18
1N4937
GOULD
biomation



8
7
6
D
C
B
+17 V UNREG.
E49
E50
Q16
R75
10 MILLI
C48
390pf
R144
10K
Q17
R66
1K
2N6211
V REF
10K
R134
47
3W
R131
300, 1W
13K
R62
13K
R100
300
1W
C50
.1
R70
10K
R67
1K
R64
5K
-15V REG
R76
10 MILLI
+6V UNREG.
E54
R141
5K
R189
5K



+15V
20.5K
+15V REG.
3/D8
R72
10K
0.5%
Co.8M
CR28
1N4152
+15V I SENSE
R54
200
3/D8
R59
10K
CR27
1N4152
+5V REG.
3/C8
+5V I SENSE
2/B1
-5.2V REG.
-5.2V I SENSE
1N4013



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COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	TO	PAR
1						1	
2						5	9000
3						7	4000
4						1	6000
5						4	6400
6						5	6400
7						1	3000
8							
9							
10						2	3000
11						1	3000
12						2	3001
13						1	3000
14						2	1200
15							
16							
17							
18							

			DRAWN J.W. CAR
			CHECKED R
			ENGINEER
			MANUFACTURING
-10	0285-0003-20	1	QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0002	P.C.B			2850 FILTER BD	FAB
-0041	INDUCTOR	L2-6			LAY
-0025	CAP	C1-7		.1uf CERAMIC	
-0410-20	CONNECTOR	J1		20 PIN RT ANG HDR N/L	
-0039	LED	DS 6-9		RED	
-0046	LED	DS 1-5		GRN	
-1006	RESISTOR	R7		10Ω 1/4W 5%	
-2701	RESISTOR	R1,2		2.7K 1/4W 5%	
-3906	" "	R3		39Ω "	
-1500	" "	R4,5		150Ω "	
-1801	" "	R6		1.8K "	
-0017	RECTIFIER	CR1,2		MR 751	

F. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	REVISED [illegible] 2758	[illegible]	[illegible]	[illegible]	
	H	REVISED PER ECO #2854	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
	C	[illegible]	[illegible]	[illegible]	[illegible]	
	D	REVISED PER ECO # [illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	E	REVISED PER ECO #2039	10-7-81	[illegible]	[illegible]	
	F	REVISED PER ECO # 2419	4-1-82	JWC	[illegible]	

	DATE
[illegible]	1-28-81
	9-4-81
	[illegible]
	[illegible]

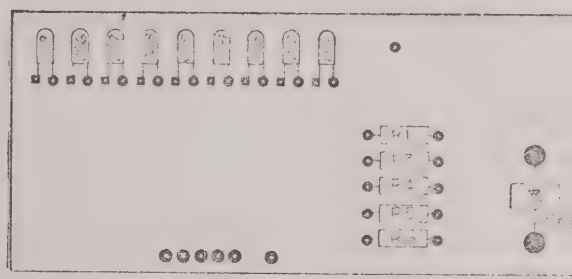
LIST OF MATERIAL

FILTER BRD

biomation

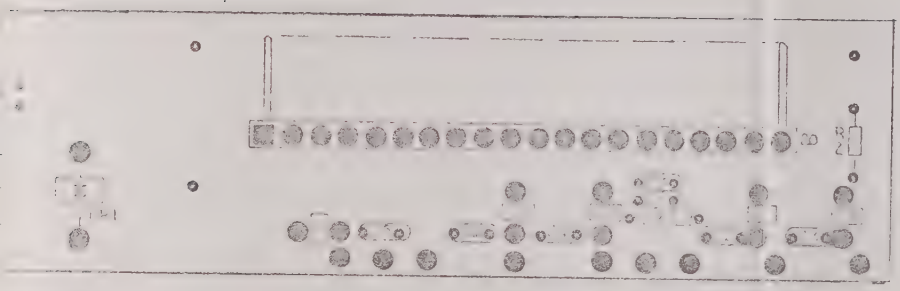
B	0285-0180	REV H

MODEL 4700 | CODE | SHEET 1 OF 1



DWG. NO 0285 0180

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	B		[illegible] PER ERN 0122			
	C	1132	[illegible] CO Nº	[illegible]		
	C		[illegible] PER ERN 0192	SWC		
	D	[illegible]	[illegible]			
	E	[illegible]	[illegible]			
	F	2419	REVISED PER ECO Nº	SWC		[illegible] 82
	G	2736	REVISED PER ECO Nº	SWC		[illegible]
	H	[illegible]	REVISED PER ECO	MW	[illegible]	[illegible]



50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING

TOLERANCE

DRAWN BY: S. ANDELL — DATE: 6-2-81

CHECKED: RG

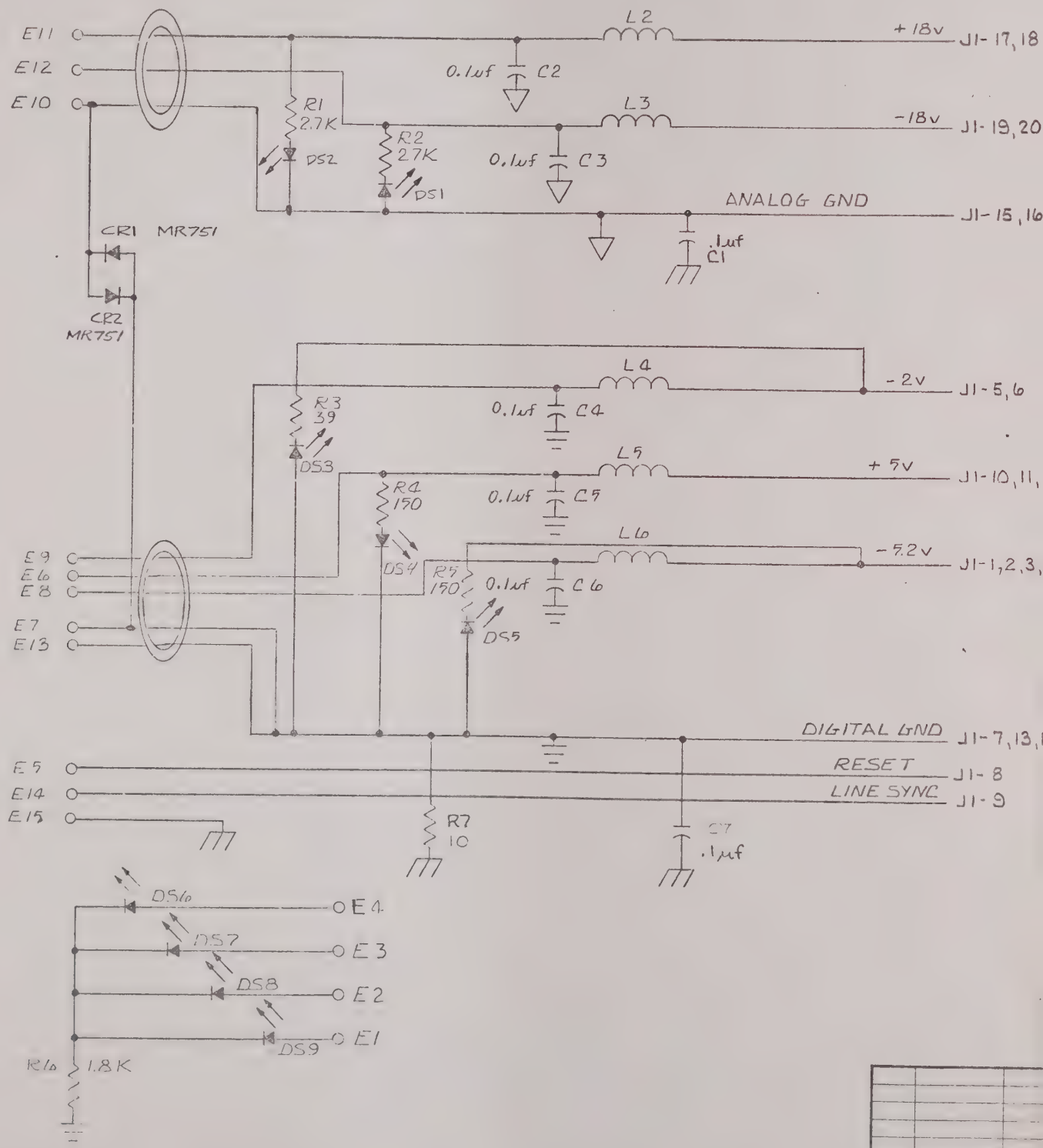
PROJ ENG

MANUFACTURING

GOULD biomation

TITLE: ASSY POWER SUPPLY FILTER BD

SCALE: 2/1 — SIZE: D — PART NUMBER: 0285-0180 — REV: H



DASH NO.	NUMBER	QTY
-10	NEXT ASSEMBLY	

MISHOP GRAPHICS ACCUPRESS REORDER NO. A4128

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTO TYPE	[illegible]		[illegible]
	[illegible]		ADDED CR1,2 DELETE UBR PILOT REL PER ERN 0122	DRS	JL	[illegible]
	C	1738	REVISED PER ECO No	JWC	RG	6-2-81
	C	—	PROD REL PER ERN #0152	JWC	RG	6-2-81
	D	1901	REVISED PER ECO	SR	RD	3-13-81
	E	2089	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	F	2674	REVISED PER ECO NO	JWC	[illegible]	7-21-82
	—	—	SKIPPED REV 'G'	[illegible]		
	H	3585A	REVISED PER ECO	[illegible]	DLW	6-17-82

NOTES:

UNLESS OTHERWISE SPECFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE IN MICRO FARRADS
3. ANALOG GROUND ▽
4. DIGITAL GROUND ⏚
5. ALL DIODES ARE: ——

DWG. NO. 0285-0181

SH 1

REV H

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

DIMENSIONAL: 1 ANGLES 20 1

HOLE SIZE: 0 599 003; 600 999 004; 1 000 1 499 005

REV | DATE

DRAWN SWCARROLL	DATE 11-18-80	GOULD biomation
CHECKED RG	6/2/81	TITLE PC [illegible] SCHEMATIC FILTER BD
PROJ. ENG		
MANUFACTURING		SCALE NONE · SIZE C · PART NUMBER 0285-018 · REV
QUALITY ASSUR		CODE 4500 · SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PAR
	-60	-50	-40	-30	-20	-10	
1							
2							
3					1		
4					1		
5					1		
6					1		
7							
8					14		
9					1		
10							
11					2		
12					1		
13					1		
14							
15					6		
16							
17							
18							

			DRAWN
			CHECKED
			ENGINEER
		1	MANUFACTURIN
		1	
		1	QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
					LM
					LM
[illegible]	FACE PLATE ASSY				LM
[illegible]175	TOP COVER				
[illegible]	LOWER COVER				
S-0173-20	HEAT SINK ASSY				LM
				TOP	[illegible]
[illegible]-0423	M/F STANDOFF				
[illegible]	[illegible] 4500				
[illegible]1	TRANSISTOR.	Q 18, 20	2N[illegible]		
[illegible]42	"	Q [illegible]	[illegible]		
[illegible]	"	Q [illegible]	[illegible]		
[illegible]016	INSULATOR	[illegible]	[illegible]		
					LM
					LM
					[illegible]

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	P	REVISED PER ECO [illegible]	[illegible]	[illegible]	[illegible]	
	Q	REVISED PER ECO [illegible]	[illegible]	[illegible]	[illegible]	
	R	REVISED PER ECO [illegible]	[illegible]	[illegible]	[illegible]	
	S	REVISED PER ECO 3[illegible]A	[illegible]	[illegible]	[illegible]	[illegible]
	D	[illegible] ECO #[illegible]	[illegible]	[illegible]	[illegible]	
	E	[illegible] ECO #[illegible]	[illegible]	[illegible]	[illegible]	
	F	REVISED PER ECO # 1827	7-1-81	[illegible]	[illegible]	

DATE

LIST OF MATERIAL

POWER SUPPLY

[illegible]

biomation

B [illegible]

MODEL 4500 | CODE | SHEET 1 OF [illegible]

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	D
20					1		
21					4		
22					1		
23					1		
24					5		
25					1		
26					1		
27					1		
28					1		
29					1		
30					2		
31					1		
32							
33							

ASSEMBLY TIME	COMPONENT LEAD SPACING

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSUR
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	[illegible]				
[illegible]	[illegible]				
-0319	SHOULDER WASHER	Q1		#4	
-0317-10	INSULATOR	Q1			
[illegible]	WASHER			#4	
19520	WIRE ASSY				LM
36-20	WIRE ASSY				LM
-0129	SWITCH	S3			
[illegible]	LABEL				
10-10	PW ASSY				LM
[illegible]	TRANSISTOR	Q7,8		2N6545	
[illegible]	PWB ASSY				LM

MARKINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	[illegible]	[illegible]	[illegible]	[illegible]	
	H	REVISED PER ECO # 1665	8.24	MB	[illegible]	
	J	REVISED PER ECO # 1859	8.24	MB	[illegible]	
	K	REVISED PER ECO # 1853	8.24	MB	[illegible]	
	L	[illegible]	[illegible]	[illegible]	[illegible]	
	M	[illegible]	[illegible]	[illegible]	[illegible]	
	N	REVISED PER ECO # 2152	[illegible]		[illegible]	

DATE [illegible]

LIST OF MATERIAL

POWER SUPPLY

TOP ASSEMBLY

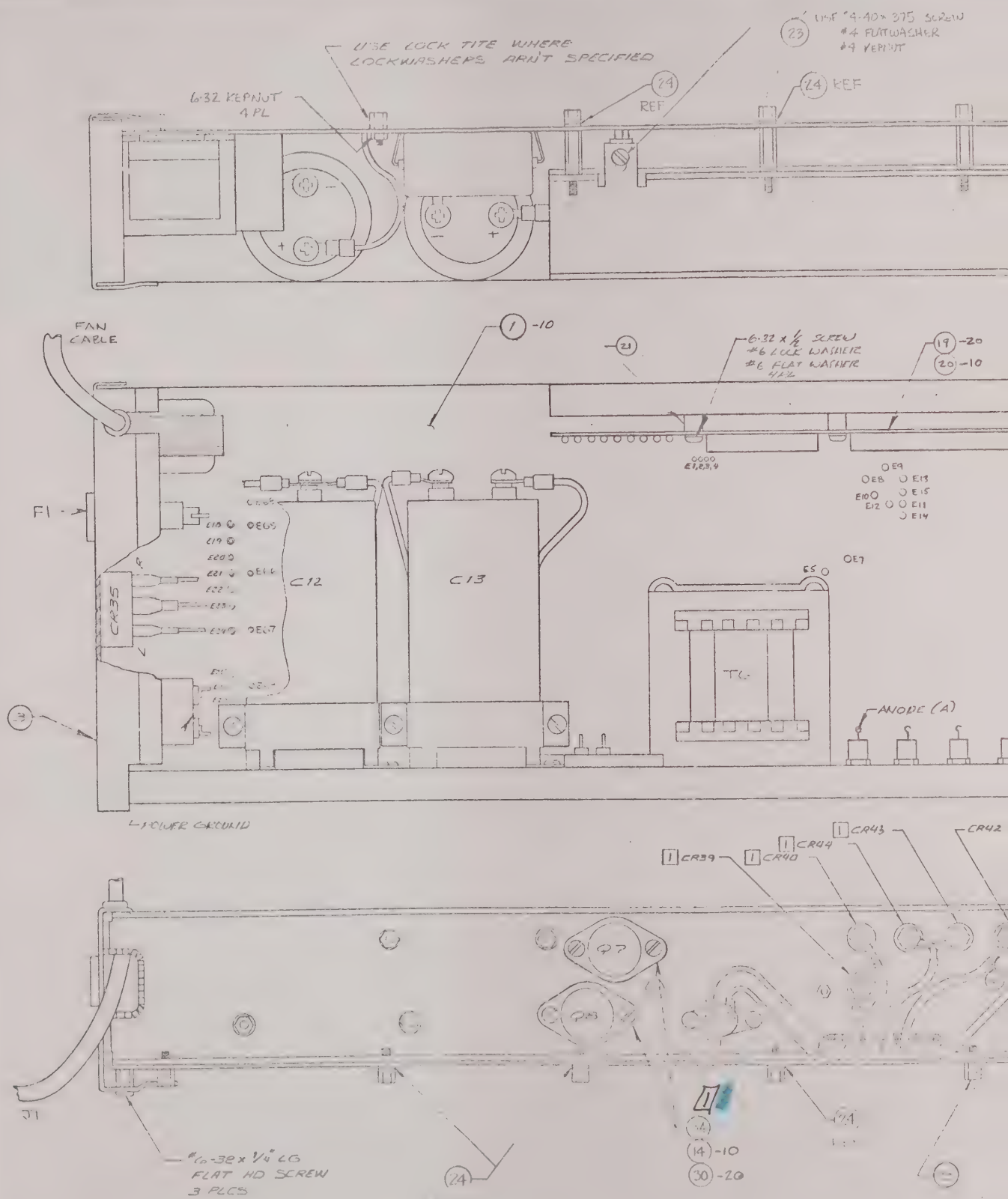
biomation

B [illegible]

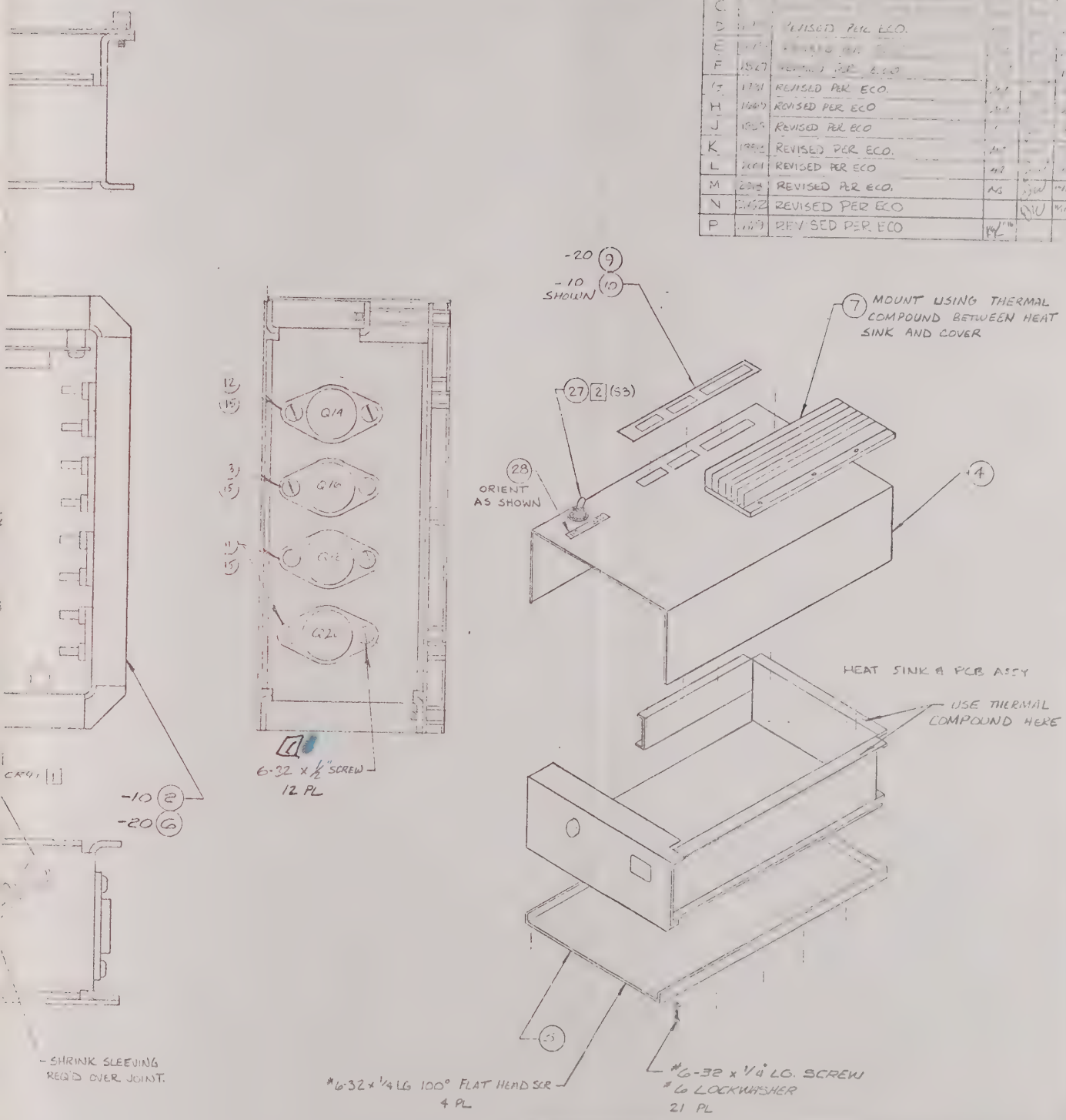
MODEL 4500

CODE

SHEET 2 OF [illegible]


USE LOCK TITE WHERE LOCKWASHERS AREN'T SPECIFIED
6-32 KEPNUT 4 PL
REF
USE 4-40 x .375 SCREW #4 FLATWASHER #4 KEPNUT
FAN CABLE
6-32 x 1/4 SCREW #6 LOCK WASHER #6 FLAT WASHER
E1,2,3,4
E9
E8
E10
E12
E13
E15
E11
E14
F1
C12
C13
CR35
E7
E5
ANODE (A)
POWER CIRCUIT
CR43
CR42
CR39
CR40
CR44
Q7
Q8
#6-32 x 1/4" LG FLAT HD SCREW 3 PLCS
Torque To no more Than 18 in lb

C					
D	[illegible]	REVISED PER ECO.			
E	[illegible]	[illegible]			
F	[illegible]	[illegible]			
G	[illegible]	REVISED PER ECO.			
H	[illegible]	REVISED PER ECO			
J	[illegible]	REVISED PER ECO			
K	[illegible]	REVISED PER ECO.			
L	[illegible]	REVISED PER ECO			
M	[illegible]	REVISED PER ECO.			
N	[illegible]	REVISED PER ECO			
P	[illegible]	REVISED PER ECO			



PART NUMBER | PART NAME

GOULD biomation

D

WIRE LIST

WIRE No.	FROM	TO	DESCRIPTION
1	E1 FILTER P.W.B.	E1 P.S. PWB	BRN
2	E2	E2	RED
3	E3	E3	ORG
4	E4	E4	YEL
5	E5	E5	LT BLU
6	—	—	
* 7	E14	E7	VIO
8	E6	E8	BRN
9	E7	E9	RED
10	E13	E10	ORG
11	E8	E11	YEL
12	E9	E12	LT BLU
13	E10	E13	BRN
14	E11	E14	RED
15	E12	E15	ORG
16	E16 P.S. PWB.	S1-1 HEAT SINK	BRN
17	E17 P.S. P.W.B.	S1-2 "	RED
18	E15 FILTER BD.	E70 P.S. PWB	VIO
20	E20 P.S. P.W.B.	CR35 (-)	BLK
21	E21	" (L)	VIO
22	E22	" (+)	YEL
23	E23	" (K)	ORG
[illegible]	—	—	
[illegible]	J1-2 EXT PLATE	E25 P.S. PWB	WHT BRN
[illegible]	E26 P.S. P.W.B.	PWR GND	GRN/YEL
27	J1-4 FACE PLATE	E27 P.S. PWB	BLK/BLU
[illegible]	E28 P.S. PWB	C12 (-) HEAT	RED
[illegible]	[illegible]	C12 (+) SINK	BRN
[illegible]	[illegible]	C13 (-) "	RED
[illegible]	[illegible]	C13 (+) "	BRN
	T6	CR42 (C) HEAT SINK	BLK [3]
	L 29	CR40 (C) "	RED
[illegible]	E 51	CR37 (A) "	RED
[illegible]	L 40	CR 31 (C)	RED
[illegible]	E60	CR39 (A)	RED
[illegible]	T6	CR31 (C)	BLK [3]
[illegible]	E 42	CR 31,40 (A)	BLU
[illegible]	L 42	CR41,42 (A)	YEL
[illegible]	E 44	CR43,44 (C)	WHT/RED
G1	E61	S1-NO	BRN
G2	E62	S1-COM	RED

* -20 ONLY

NOTES:

[1] SOLDER LUGS ON DIODES TO HAVE A MIN. OF .100 CLEARANCE TO HEAT SINK & TOP COVER.

[2] WIRES TO BE 7-10 INCHES LONG TO ALLOW FOR SERVICE LOOP. SHRINK TUBE ALL CONNECTIONS AT S3 TO PREVENT SHORTS.

[3] BLACK WIRES FROM T6 ARE INTERCHANGABLE.

S3 WIRE LIS

WIRING LIST FROM	TO
S3-1	E66
S3-2	E65
S3-3	S3-6
S3-4	E63
S3-5	E64
S3-7	E68
S3-8	E67

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE

WIRE)

S3
TOGGLE SWITCH
REAR VIEW

KEYSLOT THIS SIDE.

DO NOT SCALE DRAWING		DRAWN	DATE	GOULD biomation	
		CHECKED		TITLE	
		PROJ. ENG.			
		MANUFACTURING		SCALE	SIZE D PART NUMBER REV
DASH NO.	NUMBER	QTY	ENG. SERV.	DATE	QUALITY ASSUR.

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
1						1	600
2						1	730
3						1	730
4						1	1200
5						1	028
6						1	730
7							
8						1	028
9						1	028
10							
11							
12							
13							
14							
15							
16							
17							
18							

DASH NO.	NUMBER	QTY
-10	07[illegible]-0003[illegible]	[illegible]
-10	[illegible]-000[illegible]	1
	NEXT ASSEMBLY	

DRAWN N.

CHECKED

ENGINEER

MANUF. UR

QUALITY ASSU

R.

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0047	[illegible] CONN				
[illegible]	[illegible]				
[illegible]	[illegible]				
[illegible]	[illegible]	[illegible]		[illegible]	
[illegible]	WIRE [illegible]				LM
-0128	FUSE			6AMP 3 ALT	
[illegible]	WIRE FAB				
-0172	FACE PLATE				

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PILOT PROD REL PER ERN 0082		DCS	[illegible]	
	B	REVISED PER ECO 1522	3-20-81	MB	[illegible]	
	B	PROD REL PER ERN #0128	4-10-81	SB	RG	
	C	REVISED PER E.C.O # 1670	4-20-81	[illegible]	JL	

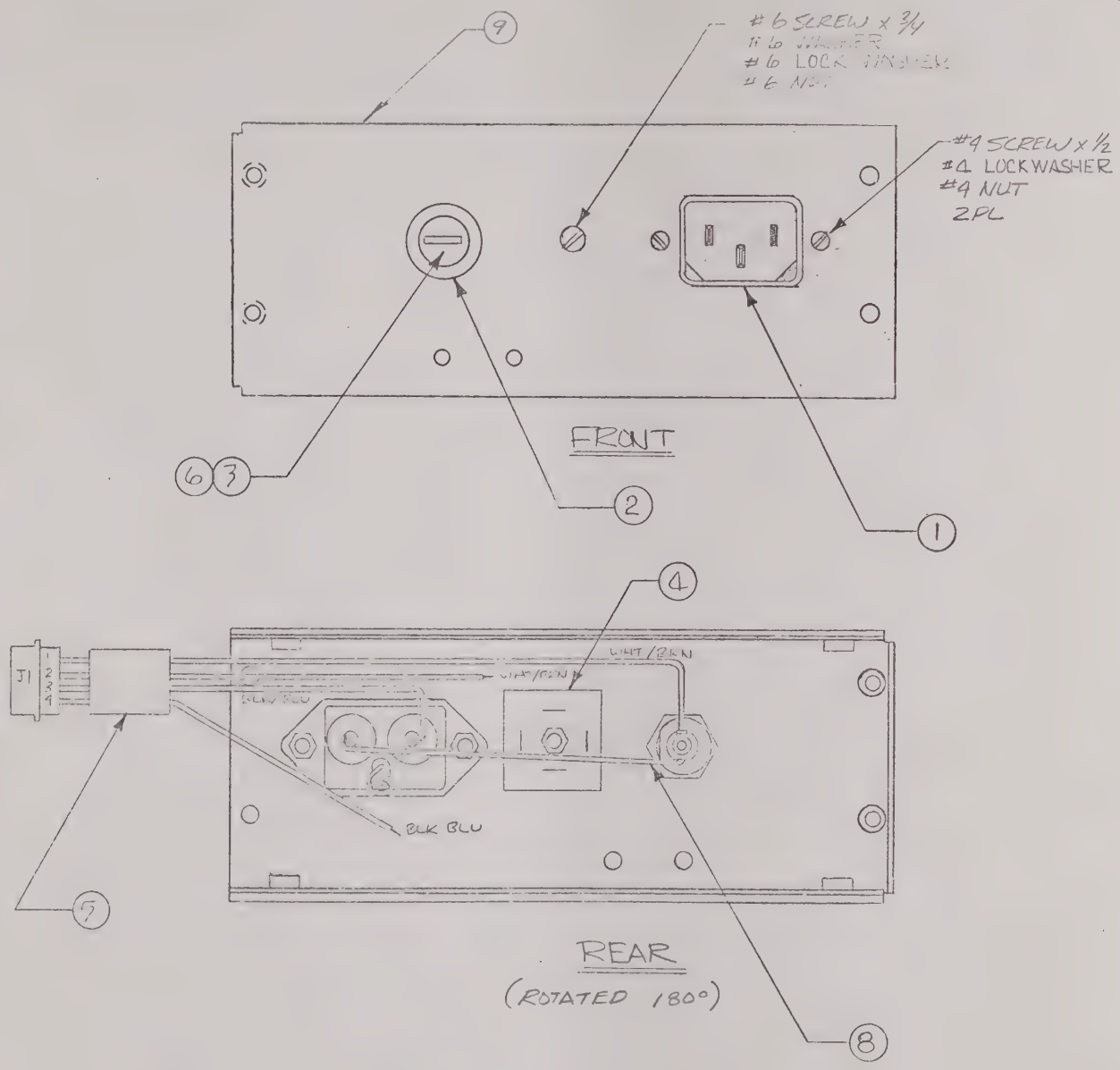
	DATE
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	
G. [illegible]	4-10-81
RANCE	[illegible]
	[illegible]

LIST OF MATERIAL
ASSEMBLY
FACE PLATE

biomation

B 0285-0156 REV C

MODEL 2850 [illegible] CODE SHEET 1 OF 1


9
#6 SCREW x 3/4
#6 WASHER
#6 LOCK WASHER
#6 NUT
#4 SCREW x 1/2
#4 LOCKWASHER
#4 NUT
2PL
FRONT
6
3
2
1

4
J1
1
2
3
4
WHT/BRN
BLK BLU
5
8
REAR
(ROTATED 180°)

2 | 1

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER ERN № 0082	JWC	RD	11-18-80
	B	1522	REVISED PER ECO.	MG	RD	3-21-81
	B		PROD REL PER ERN #0128	SR	RG	4-10-81
	C	1670	REVISED PER ECO	[illegible]	JL	4-20-81

D

C

DWG. NO. 0287-0156 SH 1 REV C

								1
-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DRAWN J W CARROLL	DATE 11-18-80
CHECKED [illegible]	4/15/81
PROJ. ENG. [illegible]	11-15-81
MANUFACTURING S Chambers	4-[illegible]
QUALITY ASSUR	
ENG. SERV [illegible]	DATE

GOULD biomation

TITLE ASSEMBLY FACE PLATE

SCALE	SIZE	PART NUMBER	REV
NONE	C	0287-0156	C

CODE [illegible] SHEET 1 OF 1

A

2 | 1

SWITCHING POWER SUPPLY
OPERATING THEORY

REFERENCE SCHEMATIC # 0285-0010

THE SWITCHING POWER SUPPLY PROVIDES FIVE VOLTAGES:

-5.2 V	AT	32 A
-2.0 V	AT	22 A
+5.0 V	AT	10 A
+15 V	AT	1.5 A
-15 V	AT	1.5 A

A. THE SWITCHING REGULATOR CONTROLS THE -5.2 V DIRECTLY AND PROVIDES THE RAW DC VOLTAGES FOR LINEAR REGULATORS WHICH CONTROL THE OTHER OUTPUTS.

B. REFERRING TO SHEET 1 OF THE SCHEMATIC, THE LINE VOLTAGE IS FILTERED AND APPLIED TO; AN OUTPUT PLUG WHICH DRIVES TWO FANS, TRANSFORMER T1, AND TO RECTIFIER CR35.

1. THE SECONDARY OUTPUT OF T1 IS RECTIFIED AND REGULATED BY Q1 AND VR1 TO SUPPLY ±15 V TO POWER THE INTERNAL CONTROL CIRCUITS OF THE SUPPLY. (THESE ARE NOT OUTPUT VOLTAGES)

C. SWITCH S3 PROVIDES 110/220 V SWITCHING FOR T1 AND THE FAN OUTPUT.

1. S3 ALSO CONTROLS THE OPERATION OF THE OUTPUT FILTERS ON CR35.

   WHEN S3 IS IN THE 110 V POSITION (OPEN) CR35, C12 AND C13 ARE CONNECTED AS A VOLTAGE DOUBLER TO PROVIDE ±150 VDC UNREGULATED.

   WITH S3 CLOSED, C12 AND C13 SIMPLY PEAK FILTER THE RECTIFIED LINE OUTPUT FROM CR35.

D. RT 1 AND RT 2 ARE THERMISTORS.

1. THEIR HIGH RESISTANCE WHEN COLD SLOWS THE SURGE OF CURRENT TO CHARGE C12 AND C13 AT TURN-ON.
2. UNDER NORMAL OPERATING CONDITIONS, C12 AND C13 DISCHARGE VERY SLOWLY AFTER POWER-DOWN.
3. WHEN THE COVER IS REMOVED FOR MAINTENANCE, S2 OPENS, ENABLING Q4 WHICH ACTS AS A FAST DISCHARGE PATH WHEN POWER IS TURNED OFF.
4. OPTO-ISOLATOR U14 HOLDS Q4 OFF WHEN POWER IS ON.
5. THIS FAST DISCHARGE IS FOR PROTECTION OF SERVICE PERSONNEL.

E. CR4 AND CR5 ARE "TRANSORBS" WHICH PROTECT THE SWITCHING TRANSISTORS FROM LINE TRANSIENTS.

1. IF THE UNIT IS PLUGGED INTO 220 V WHEN S3 IS IN THE 110 V POSITION, THE "TRANSORBS" WILL SHORT, BLOWING THE FUSE, BUT PROTECTING THE SWITCHING TRANSISTORS.

F. THE SWITCHING REGULATOR IS AT LOCATION U8, A TL 494.

1. AN INTERNAL 40 KHz OSCILLATOR ALTERNATELY PULSES THE OUTPUTS AT U8 PINS 8 AND 11.

   THESE PULSES ARE THE BASE DRIVE SIGNALS FOR SWITCHING TRANSISTORS Q7 AND Q8.

2. U8 VARYS THE OUTPUT PULSE WIDTH (AND THUS THE "ON TIME" OF Q7 & Q8) TO MAINTAIN CONSTANT FEEDBACK VOLTAGE FROM THE -5.2 VDC OUTPUT OF THE T6 SECONDARY RECTIFIERS.
3. Q5, Q6, T4, T5 AND ASSCOCIATED COMPONENTS SHAPE AND COUPLE THE DRIVE SIGNALS TO THE BASES OF Q7 AND Q8.
4. Q7 AND Q8 SWITCH THE PRIMARY OF T6 BETWEEN PLUS AND MINUS 150 VDC AT A 20 KHz RATE.

THIS HIGH FREQUENCY ALLOWS T6 TO BE RELATIVELY SMALL COMPARED TO A 60 HZ TRANSFORMER AND ALLOWS FOR PHYSICALLY SMALLER COMPONENTS FOR FILTERING THE RECTIFIED OUTPUTS.

5. T7, CR6, CR7, R17, R18, AND C14 ACT AS A SENSOR FOR PRIMARY CURRENT.

6. THE VOLTAGE ON C14 IS PROPORTIONAL TO THE AVERAGE CURRENT IN THE PRIMARY WINDING.

7. T6 HAS THREE SECONDARY WINDINGS WHO'S OUTPUTS ARE RECTIFIED AND FILTERED TO PROVIDE 5 DC VOLTAGES:

- 5.20 V	REGULATED
+ 6.00 V	UNREGULATED
- 3.00 V	UNREGULATED
-17.00 V	UNREGULATED
+17.00 V	UNREGULATED

8. THE REGULATED -5.2 V OUTPUT IS FED TO THE OUTPUT OF THE SUPPLY VIA THE FILTER BOARD AFTER PASSING THROUGH R90, A 1.2 MILLI-OHM RESISTOR.

9. R90 AND R95 ACT AS A CURRENT SENSOR.

   THE VOLTAGE DIFFERENCE BETWEEN THE BOTTOM OF R95 AND THE OUTPUT SIDE OF R90 IS PROPORTIONAL TO THE CURRENT DRAWN FROM THE -5.2 V SUPPLY.

10. THE 4 UNREGULATED VOLTAGES FROM THE SECONDARY RECTIFIERS GO TO LINEAR REGULATORS, SHOWN ON SHEET 3 OF THE SCHEMATIC, WHICH PROVIDES +5.0 V, -2.0 V, AND ±15 VDC.

11. THE OUTPUTS OF THE REGULATORS ARE ROUTED THROUGH CURRENT SENSE NETWORKS SIMILAR TO THE ONE ON THE -5.2 V SUPPLY AND THEN TO THE OUTPUTS ON THE FILTER BOARD.

G. THE POWER SUPPLY PROTECTION CIRCUITS ARE SHOWN ON SHEET 4 OF THE SCHEMATIC.

1. THE SUPPLY IS DESIGNED TO TURN ITSELF OFF IN CASE OF OVER TEMPERATURE, HIGH OR LOW LINE VOLTAGE, PRIMARY OVER CURRENT, OR OVER CURRENT ON ANY OF THE 5 OUTPUT VOLTAGES.

2. THE OUTPUTS OF U3 AND U4 WILL GO HIGH ANY TIME THE CURRENT THROUGH THE SENSE RESISTORS ON THE REGULATED SUPPLIES EXCEEDS THE PRESET THRESHOLDS.

   THIS HIGH IS LATCHED IN U2 AND THEN U5 BY THE 40 KHZ CLOCK FROM THE TL494.

3. U5 PIN 13 GOING HIGH RESETS U6, CAUSING U6 PIN 8 TO GO HIGH FOR .4 SECONDS

4. A HIGH ON ANY OF THE INPUTS OF U11 CAUSES "SUPPLY ENABLE" TO GO FALSE, SHUTTING OFF THE TL494 OUTPUTS.

5. AFTER THE .4 SECOND PULSE GOES AWAY, THE SUPPLY WILL ATTEMPT TO RE-START BUT WILL SHUT DOWN AGAIN IF THE FAILURE STILL EXISTS.

6. WHEN A PRIMARY OVER-CURRENT CONDITION IS DETECTED, U9-1 GOES HIGH SETTING U5-13 HIGH RESETTING U6 WHICH AGAIN ALLOWS THE SUPPLY TO ATTEMPT A RE-START AFTER .4 SEC.

7. U9 PINS 8 & 7 GO LOW FOR INPUT OVER AND UNDER VOLTAGE, RESPECTIVELY.

   EITHER OF THESE GOING HIGH CAUSES U10-3 TO GO HIGH.

8. U10-3 DRIVES U-11 DIRECTLY AS DOES THE OVERTEMPERATURE SENSOR, S1.

   THUS, THERE IS NO AUTOMATIC RE-START ATTEMPT FOR THESE FAILURE CONDITIONS.

H. U10, Q10 AND THEIR ASSCOCIATED COMPONENTS PROVIDE A RESET SIGNAL TO THE MPU IN THE K101 EACH TIME THE SUPPLY SHUTS OFF OR TURNS ON AND WHEN THE POWER IS TURNED OFF.

THE K500 DOES NOT USE THIS SIGNAL.

THE K101 USES THE POWER-DOWN RESET TO FASCILITATE SAVING THE CURRENT INSTRUMENT STATUS ON TURN-OFF.

Section 10

MEASUREMENT CONFIDENCE

10.1 INTRODUCTION

The K101-D has three self-diagnostic routines to give you confidence that it is operating correctly: Probe Test, Power Up Test, and Self-Test. Successful completion of these tests ensures that your K101-D is operating correctly and that the measurements it makes are valid. If there is a problem in the analyzer, these tests help you to quickly identify the problem.

a. **Probe Test:** The two clock and eight sample inputs of each probe can be quickly tested for correct detection of signal inputs by a built-in Probe Test socket which generates a known ring-counter pattern and clocking signals. Besides physically checking a probe's inputs, Probe Test can be used to explore and understand the operation of the K101-D itself.

b. **Power Up Test:** When the K101-D is turned on, a series of tests is automatically performed. The unit's ROM, RAM, power supply, CMOS RAM, USARTs, and keyboard are checked for correct operation.

c. **Self-Test:** For maximum confidence in the K101-D's operation, any of a series of detailed diagnostic tests may be performed. There are also troubleshooting test routines to help you debug any instrument error that may appear. Running Self-Test before calling the factory or shipping your instrument back for repair could save you a lot of time, trouble, and money.

10.2 PROBE TEST

The Probe Test discussion is intended to familiarize you with the operation of the K101-D, and verify that the equipment is working properly. The examples in this section are related to the A section inputs, and are summarized in Table 10-1. These examples are designed to be performed sequentially. The directions for creating a specific setup assume you will only need to make changes from the preceeding setup. Where appropriate, setup guides and illustrations of the desired setup screens are included to help you check that your setup is correct.

Turn the power on. Once the power up test sequence is complete, press **SHIFT, RECALL** to initialize all setups to their default values.

> Note
>
> If you make a mistake on a particular example you can start over by using the **SHIFT/RECALL** keys.

10.2.1 PROBE CONNECTION

Plug the SECTION A INPUTS CLK J, K, F . . . 8 probe cable into its front panel input and the pod into the Probe Test socket. The probe PC board key slot should be on your left and the pod labels facing up. To avoid getting noise on the other inputs, plug all the other probe cables into their appropriate front panel section inputs.

Table 10-1. Probe Test Exercises

Topic	Paragraph Number
Probe Connection	10.2.1
Polarity and Threshold:	
a. Fixed TTL	10.2.2.1
b. Fixed ECL	10.2.2.2
c. Stabilize pattern	10.2.2.3
d. Variable threshold	10.2.2.4
e. Negative polarity	10.2.2.5
Data Format:	
a. Delete inputs	10.2.3.1
b. Repeat inputs	10.2.3.2
c. Fixed format	10.2.3.3
Clock and Input:	
a. Sample internally	10.2.4.1
b. Sample -- single external clock	10.2.4.2
c. Sample -- multiple external clocks	10.2.4.3
d. Latch (Enable) -- combination	10.2.4.4
e. Demux -- single enable input	10.2.4.5
f. Demux -- combination enable inputs	10.2.4.6
Basic Trace Control:	
a. Fill MEM from anywhere	10.2.5.1
b. Record immediately after event	10.2.5.2
c. Record immediately before event	10.2.5.3
d. Record around an event	10.2.5.4
e. Record long after event	10.2.5.5
f. Record from here to there	10.2.5.6
g. Don't record from here to there	10.2.5.7

Table 10-1. Probe Test Exercises (Cont'd)

Topic	Paragraph Number
h. Selectively record -- n times	10.2.5.8
i. Follow a path -- then record	10.2.5.9
j. Record -- then follow a path	10.2.5.10
k. Check for event 1 or 2	10.2.5.11
l. Take same path -- ignore events	10.2.5.12
m. Check timing between two events	10.2.5.13
n. Monitor for correct operation	10.2.5.14
Advanced Trace Control:	
a. Continuous check -- path and timing	10.2.6.1
b. Trace independent of execution path	10.2.6.2
c. End level break point	10.2.6.3
d. Segments, patterns, and total trace time	10.2.6.4
Record:	
a. Manual arm	10.2.7.1
b. Auto arm	10.2.7.2
c. Limiting the count	10.2.7.3
d. Stop if A ≠ B	10.2.7.4
e. Auto Stop if A = B	10.2.7.5
f. Auto Stop if A ≠ B within limits	10.2.7.6
g. Auto Stop if A = B within limits	10.2.7.7

10.2.2 POLARITY AND THRESHOLD

10.2.2.1 **Fixed TTL Threshold**

SET UP: None required. Uses the default values.

RECORD: Press ARM . This will arm (enable) recording of data.

REVIEW: Display timing data page 4. Press TIMING , PAGE 4 four times to reach page 4.

You should see all zeros on all inputs (see Figure 10-1). This is because the Probe Test signals are generated by ECL logic, which typically uses a threshold of -1.30 volts (well below the default TTL value of +1.4 volts).

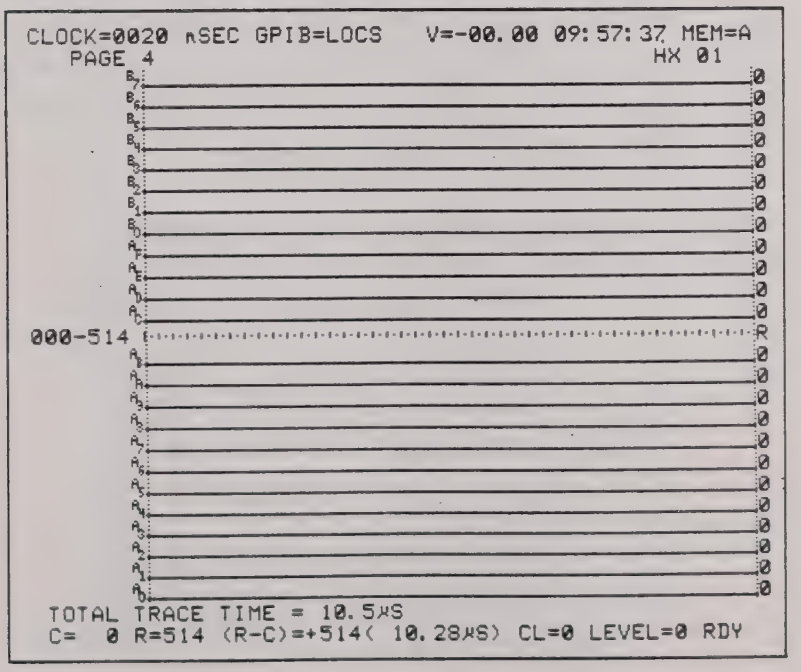


Figure 10-1. Resulting Probe Test Recording Using a TTL Threshold.

10.2.2.2 **Fixed ECL Threshold**

SET UP: Press INPUT MODE.

Change the threshold for inputs AF through A8 to ECL by moving the blinking cursor to the AF-A8 line of the Input Mode display and change TTL to ECL.

Press △ three times, ▷ , 9 (EBCDIC / ECL).

RECORD: Press ARM.

REVIEW: Press TIMING.

A staircase pattern of pulses should be seen (Figure 10-2). This pattern may start anywhere on the screen because of the default trace control program, "Fill Memory with Samples from Anywhere in the Data Stream." Use the Control and Reference Cursors to measure the characteristic total trace time of 10.5 microseconds and pulse width of 0.9 microseconds.

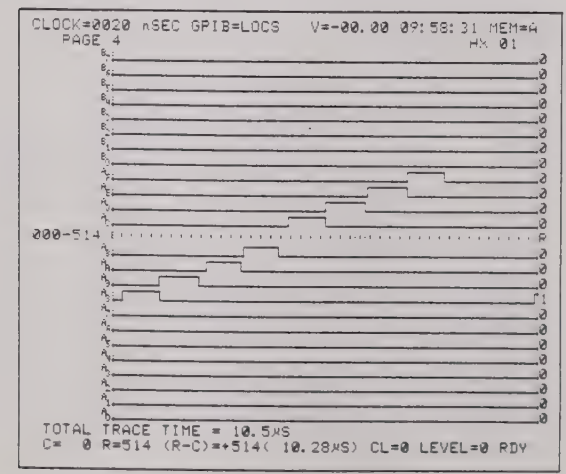


Figure 10-2. Typical Probe Test Recording Using an ECL Threshold.

10.2.2.3 **Stabilize Pattern**

SET UP: Obtain one full pattern that starts in the same location every time. Change the S word recognizer to S = xxxx xxxx 01xx.

Press TRACE CONTROL .

Move the cursor to S. Press ▽ SET twice, ◁ SET eight times, then 0 (Hx1) G, 1 (Hx3) H.

RECORD: Press ARM .

REVIEW: Press TIMING .

The display should look like Figure 10-3. The pattern will begin in the same location every recording through the use of the trace control command STOP IF DATA = S AND SAMPLE COUNT DELAY WHERE S = XXXX XXXX 01XX and DELAY = DEC 515 CLOCKS. Note that the total trace time is greater than 10.5 microseconds because of the extra time spent waiting for the specified trace control STOP condition to come true.

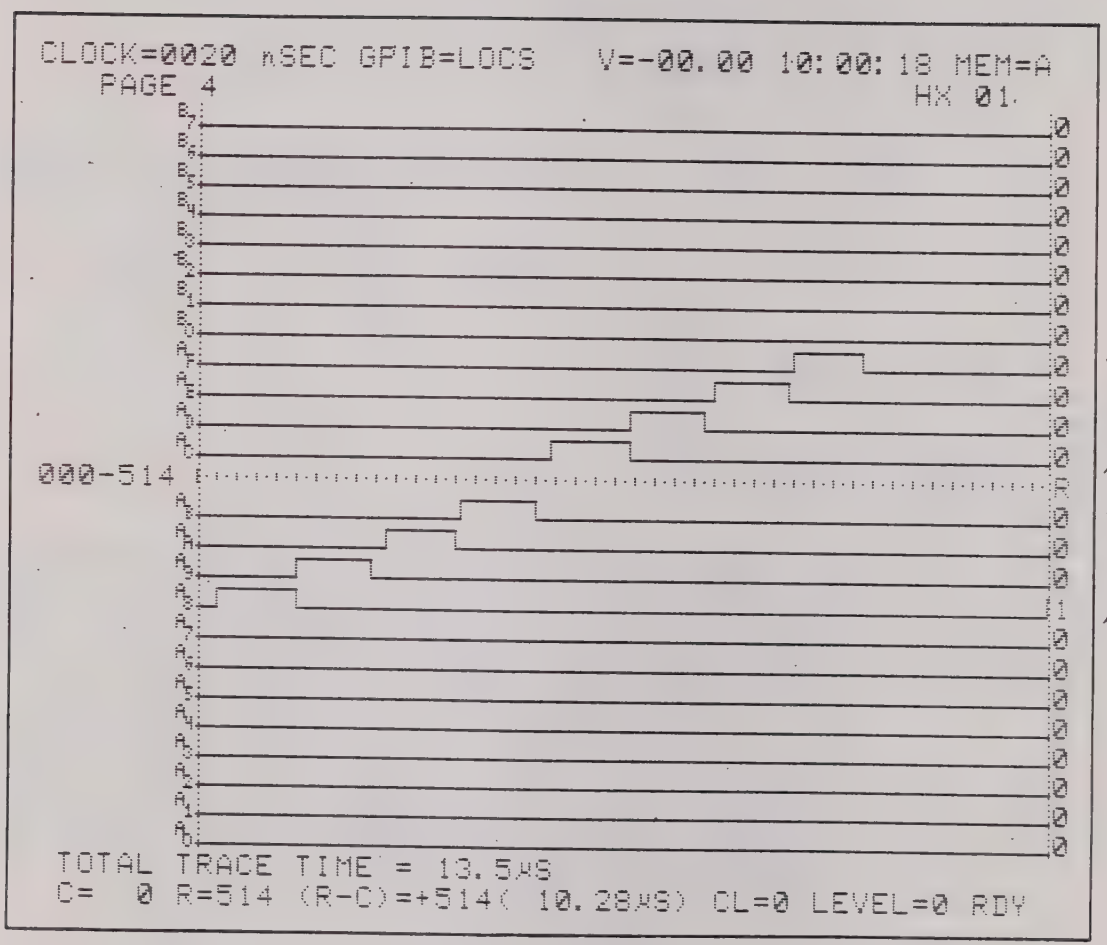


Figure 10-3. Fixed Location Pattern.

10.2.2.4 **Variable Threshold**

SET UP: Display the Input Mode screen.

Press [INPUT MODE] .

Change the threshold for inputs AF through A8 to VARA.

Press [△] three times, [+ ▷] , [ASCII A Q] .

Change the value to something other than -1.30 volts such as -1.00 volts. Move the cursor to the numerical value and enter the digits (which are entered sequentially).

Press [+ ▷] , [FALSE −] , [Hx3 1 H] , [Hx1 0 G] , [Hx1 0 G] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

Look for any difference in the pattern such as missing or shortened (<0.9 microsecond) pulses (check pulse width with the cursors), as shown in Figures 10-4 and 10-5, respectively. In Figure 10-4 note that the pulses that do not exceed the threshold will not be detected (threshold = 0.00 volts). In Figure 10-5 note that slow rise and fall times cause only that portion of the pulse that exceeds the threshold to be detected (threshold = +0.50 volts). If you see no irregularities, go back and change the threshold to some other value, record, and review again. Repeat this process until you perceive a noticeable change.

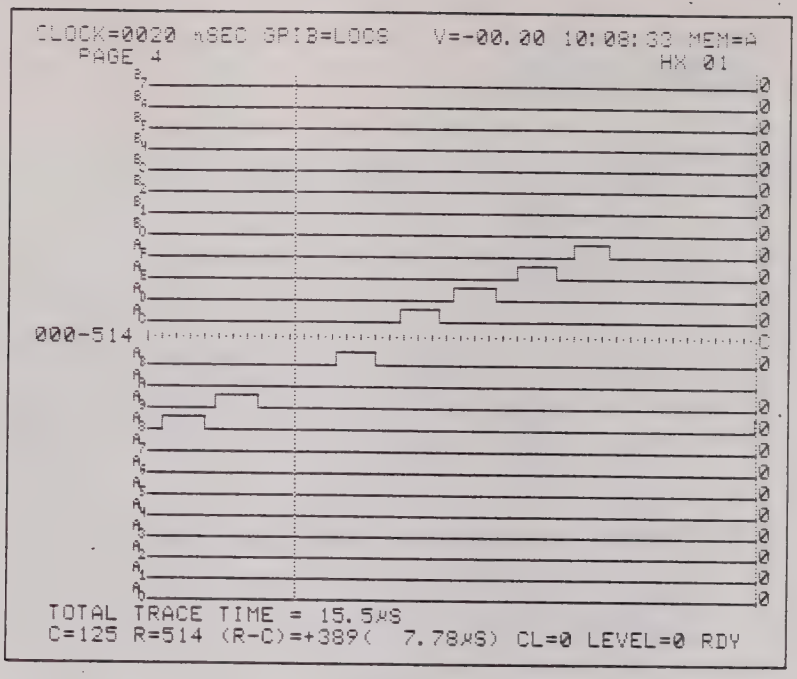


Figure 10-4. Pattern Changes with Threshold Changes.

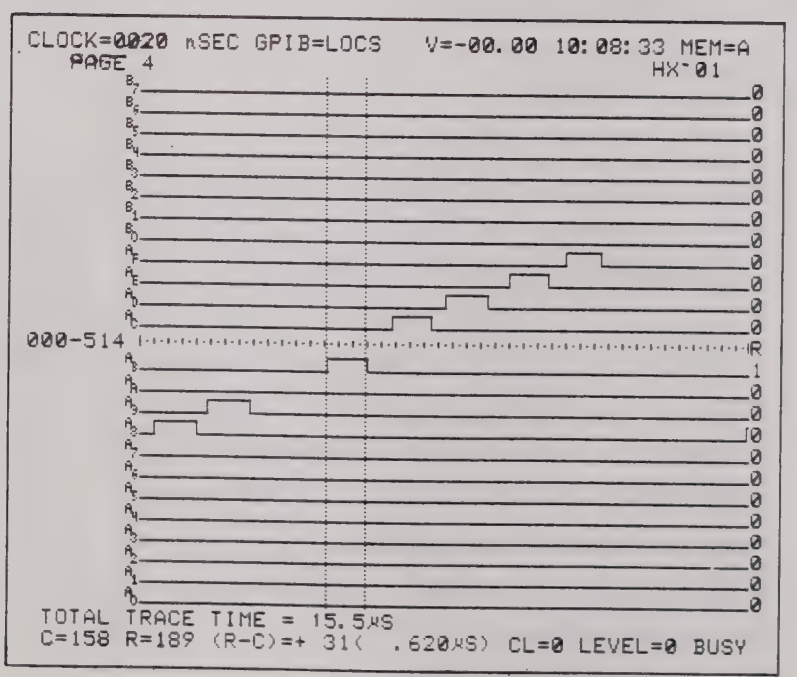


Figure 10-5. Effect of Rise and Fall Time.

10.2.2.5 **Negative Polarity**

SET UP: Display logic polarity screen. Press LOGIC POLARITY .

Change the polarity of inputs AF through A8 to negative.

Press ▽ SET twice, FALSE − eight times.

Return threshold to ECL.

Press INPUT MODE , △ three times, ▷ , EBCDIC 9 ECL .

RECORD: Press ARM .

REVIEW: Press TIMING .

The trace level status will say LEVEL = 0 BUSY. (The displayed timing information is from the previous recording.) Trace control looks for 01 (hex) but never sees it because of the reversed polarity. Check what information is flowing from memory M to memory A.

Press M→A .

The display shows what information was flowing into memory and through trace control (see Figure 10-6). With negative polarity, positive-going pulses are a logical "0." The total trace time reading reflects the time between your pressing of the **ARM** and **M -> A** keys. Move the Control or Reference Cursor through the pulses (by holding down the appropriate cursor keys) while watching the binary cursor readout. Stop when the cursor is at the A8 input pulse. Note that for inputs AF through A8, a positive-going pulse is detected and represented as a logical "0," which is the definition of negative polarity.

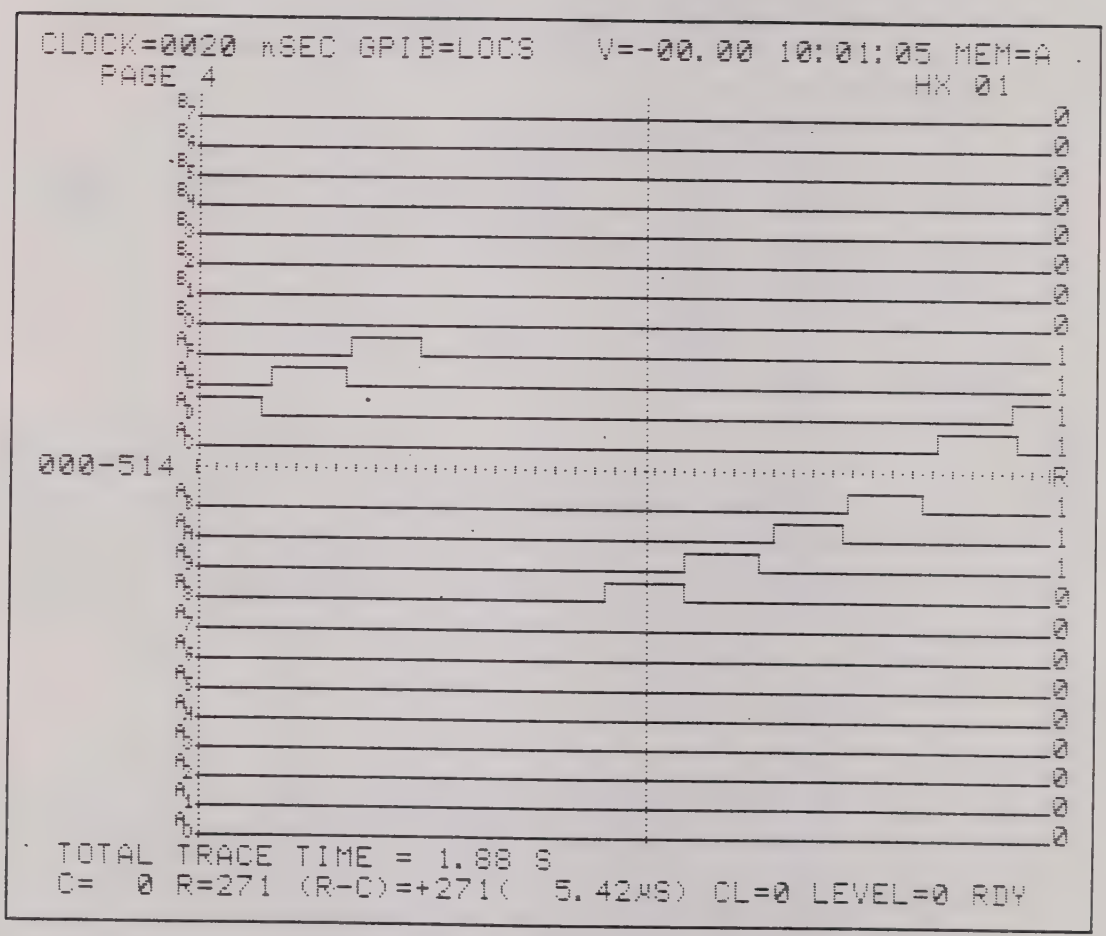


Figure 10-6. Information Flow.

10.2.3 DATA FORMAT

10.2.3.1 **Delete Inputs**

SET UP: See setup guide in Figure 10-7. Display Clock Select screen.

Press CLOCK SELECT .

Select the first option. Press Hx3 1 H .

Move to the master clock line. Press ▽ SET twice.

Select second option and move cursor. Press Hx6 2 ' , ▷ twice.

Select first option. Press Hx3 -1 H .

Select Logic Polarity display. Press LOGIC POLARITY .

Move cursor to A section. Press ▽ SET twice.

Enter plus polarity for first eight inputs. Press TRUE + eight times.

The Clock Select and Trace Control displays should now look like Figures 10-8 and 10-9.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 31 OF ___ DATE _____

QUICK KEY (...3...) DATA FORMAT MIXED USER SEQN.

RADIX:	H H H H H H H H H H H H
MSB	
I 6	
D N 5	
A P 4	
T U 3	$C_F C_E C_D C_C$ $B_F B_E B_D B_C$ $A_F A_E A_D A_C$
A T 2	$C_B C_A C_9 C_8$ $B_B B_A B_9 B_8$ $A_B A_A A_9 A_8$
S 1	$C_7 C_6 C_5 C_4$ $B_7 B_6 B_5 B_4$ $A_7 A_6 A_5 A_4$
LSB	$C_3 C_2 C_1 C_0$ $B_3 B_2 B_1 B_0$ $A_3 A_2 A_1 A_0$

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = 0
1	Always
2	Never
3	If DATA = 0 and Sample Count - Delay
4	If DATA = 0 and Sample Count - Delay
5	If DATA = 0 and Sample Count = Delay
6	If DATA = 0 and Sample Count ≠ Delay
7	If DATA = 0 and Sample Count - ≠ Delay
8	If DATA = 0 and Sample Count - Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX) CLOCKS (0-65 K) (CLOCKS/A PATTERNS) END LEVEL F (O-F) — COMMENTS

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X X X X X X X X X X X

(2) JUMP TO 0 (O-F) NEVER
J = X X X X X X X X X X X X

(2) ADVANCE NEVER
A = X X X X X X X X X X X X

(1) TRACE ALWAYS
T = X X X X X X X X X X X X

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(____) STOP
S =
(____) JUMP TO ___ (O-F)
J =
(____) ADVANCE
A =
(____) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(____) STOP
S =
(____) JUMP TO ___ (O-F)
J =
(____) ADVANCE
A =
(____) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(____) STOP
S =
(____) JUMP TO ___ (O-F)
J =
(____) ADVANCE
A =
(____) TRACE
T =

Figure 10-7. Setup (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 3.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (...1...) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ 1) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence
1	OCTAL — Fixed octal format & CF-A0 sequence
2	BINARY — Fixed binary format & CF-A0 sequence
3	MIXED USER SEQR — Any radix, any sequence
4	MIXED CF-A0 SEQR — Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 assembler; OR
5	DEVICE NOT AVAILABLE — No RTE-816 assembler

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTION
0	INTERNAL — All sections are sampled at the internal clock rate. Section A = Section B = Section C = internal clock period.
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master external.
2	EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B, and/or Section C = Master external or internal clock period or 10ns.
4	MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B, and/or Section C = Master external or internal or 10ns.
5	INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and/or Section C = internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (...0...) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-612, R: 0-612)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-7. Setup (Sheet 2 of 2).

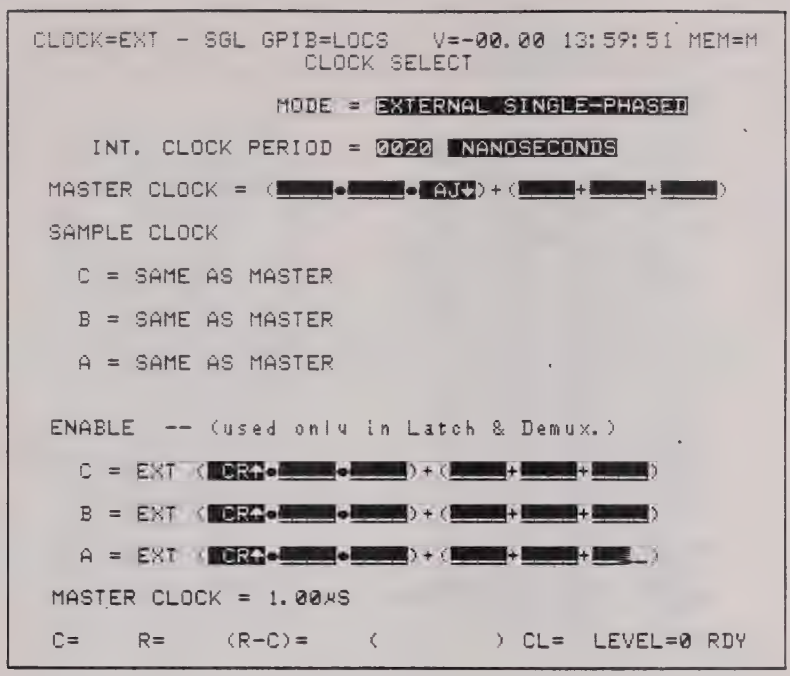


Figure 10-8. Clock Select for Delete Example.

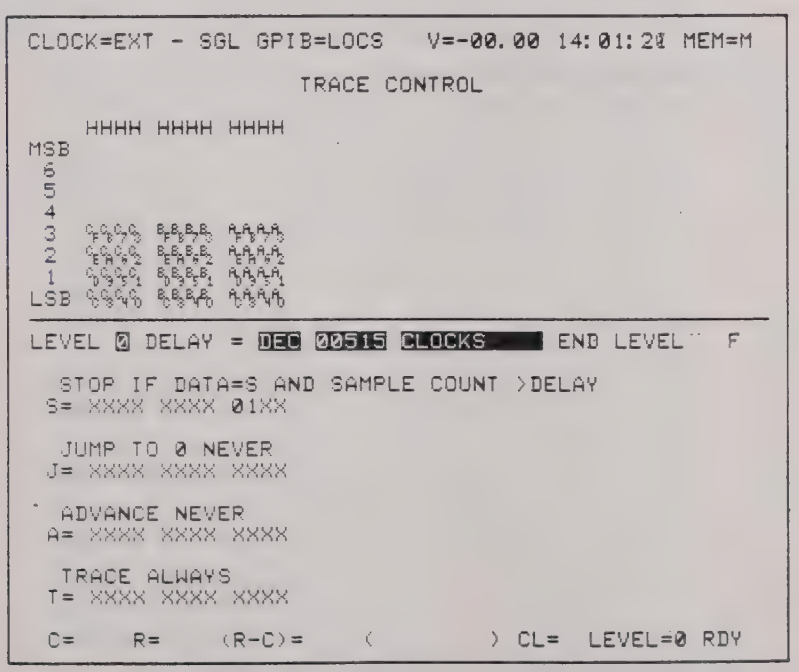


Figure 10-9. Trace Control for Delete Example.

RECORD: Press ARM .

REVIEW: Display the synchronously recorded pattern.

Press TIMING , Hx12 3 .

Display the data. Press DATA .

The display should look like Figure 10-10 which is full data display for inputs AF through A8, probe test recording. . (If any columns are filled with Fs, it means that the probe is not plugged into the front panel.)

Display the corresponding graph (see Figure 10-11) which is based on the original data format. Since the hex value of each 12-character word is close to zero, only a baseline can be seen.

```
CLOCK=EXT - SGL GPIB=LOCS   V=-00.00 10:16:24 MEM=A

     HHHH HHHH HHHH                HHHH HHHH HHHH
000C0000 0000 0000          024 0000 0000 0800
001 0000 0000 0100          025 0000 0000 1000
002 0000 0000 0200          026 0000 0000 2000
003 0000 0000 0400          027 0000 0000 4000
004 0000 0000 0800          028 0000 0000 8000
005 0000 0000 1000          029 0000 0000 0000
006 0000 0000 2000          030 0000 0000 0000
007 0000 0000 4000          031 0000 0000 0100
008 0000 0000 8000          032 0000 0000 0200
009 0000 0000 0000          033 0000 0000 0400
010 0000 0000 0000          034 0000 0000 0800
011 0000 0000 0100          035 0000 0000 1000
012 0000 0000 0200          036 0000 0000 2000
013 0000 0000 0400          037 0000 0000 4000
014 0000 0000 0800          038 0000 0000 8000
015 0000 0000 1000          039 0000 0000 0000
016 0000 0000 2000          040 0000 0000 0000
017 0000 0000 4000          041 0000 0000 0100
018 0000 0000 8000          042 0000 0000 0200
019 0000 0000 0000          043 0000 0000 0400
020 0000 0000 0000          044 0000 0000 0800
021 0000 0000 0100          045 0000 0000 1000
022 0000 0000 0200          046 0000 0000 2000
023 0000 0000 0400          047 0000 0000 4000

  C=  0 R=514 (R-C)=+514(         ) CL=0 LEVEL=0 RDY
```

Figure 10-10. Data Display, Probe Inputs AF through A8.

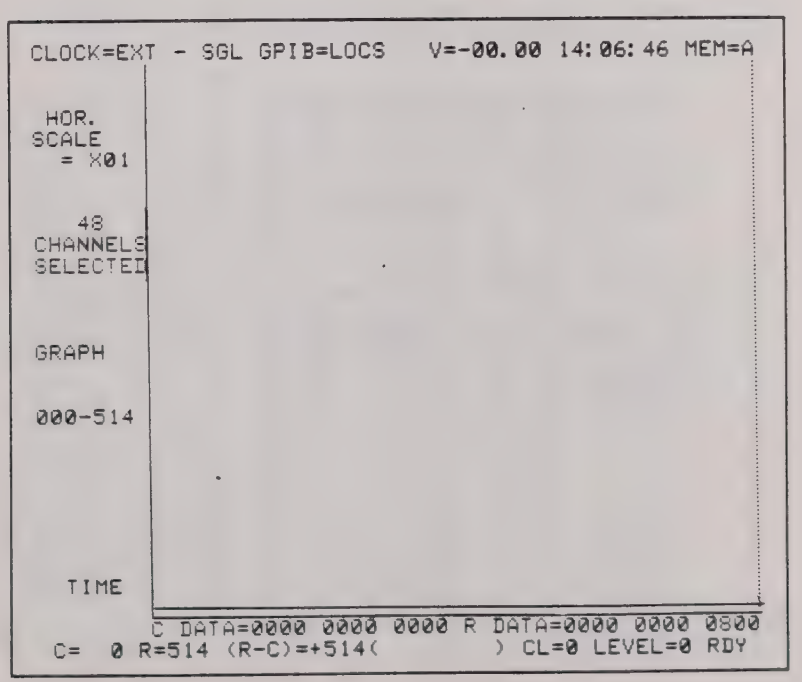


Figure 10-11. Graph of Data of Figure 10-10.

Press GRAPH .

Display the data format. Press DATA FORMAT .

Delete all inputs except AF through A8.

Press ▽ SET , DELETE ten times, ▷ twice, DELETE twice.

Check that the word recognizer formats have correspondingly changed.

Press TRACE CONTROL (see Figure 10-12). Note that changing the data format also changes the trace control's word recognizer format.

Press DATA (see Figure 10-13).

Check the new graph format.

Press GRAPH (see Figure 10-14).

Note the number of channels selected and that changing the data format changes the input channels that are graphed.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 10:19:07 MEM=M

                    TRACE CONTROL

    HH
MSB
 6
 5
 4
 3
 2
 1
LSB

LEVEL 0 DELAY = DEC 00515 CLOCKS      END LEVEL   F

  STOP IF DATA=S AND SAMPLE COUNT >DELAY
 S= 01

  JUMP TO 0 NEVER
 J= XX

  ADVANCE NEVER
 A= XX

  TRACE ALWAYS
 T= XX

 C=     R=     (R-C)=     (          ) CL=  LEVEL=0 RDY
```

Figure 10-12. Data Format/Word Recognizer Changes.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 10:16:24 MEM=A

    HH       HH       HH       HH       HH       HH
000C00   024 08   048 80   072 02   096 20   120 00
001 01   025 10   049 00   073 04   097 40   121 01
002 02   026 20   050 00   074 08   098 80   122 02
003 04   027 40   051 01   075 10   099 00   123 04
004 08   028 80   052 02   076 20   100 00   124 08
005 10   029 00   053 04   077 40   101 01   125 10
006 20   030 00   054 08   078 80   102 02   126 20
007 40   031 01   055 10   079 00   103 04   127 40
008 80   032 02   056 20   080 00   104 08   128 80
009 00   033 04   057 40   081 01   105 10   129 00
010 00   034 08   058 80   082 02   106 20   130 00
011 01   035 10   059 00   083 04   107 40   131 01
012 02   036 20   060 00   084 08   108 80   132 02
013 04   037 40   061 01   085 10   109 00   133 04
014 08   038 80   062 02   086 20   110 00   134 08
015 10   039 00   063 04   087 40   111 01   135 10
016 20   040 00   064 08   088 80   112 02   136 20
017 40   041 01   065 10   089 00   113 04   137 40
018 80   042 02   066 20   090 00   114 08   138 80
019 00   043 04   067 40   091 01   115 10   139 00
020 00   044 08   068 80   092 02   116 20   140 00
021 01   045 10   069 00   093 04   117 40   141 01
022 02   046 20   070 00   094 08   118 80   142 02
023 04   047 40   071 01   095 10   119 00   143 04

 C=  0 R=514 (R-C)=+514(          ) CL=0 LEVEL=0 RDY
```

Figure 10-13. New Data Display for Figure 10-12 Data Format.

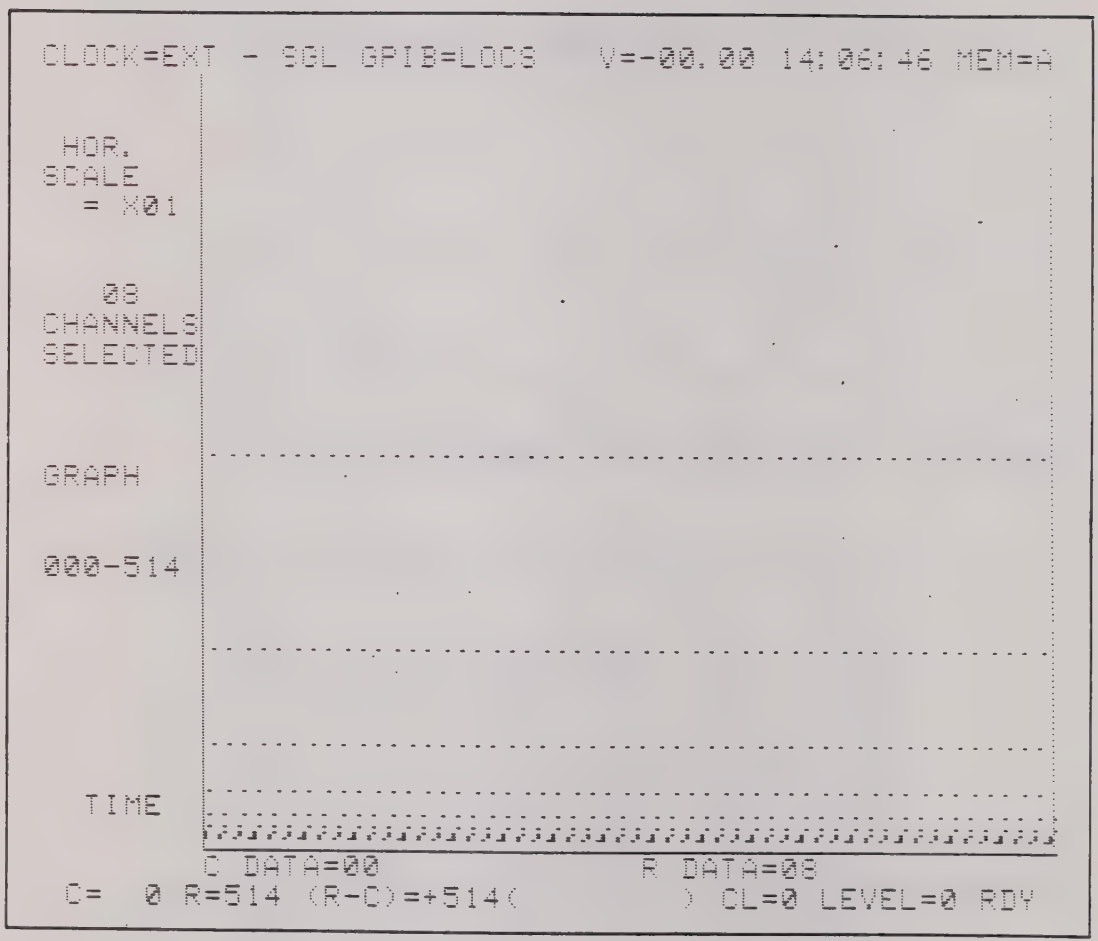


Figure 10-14. Change of Input Channel Graphed.

10.2.3.2 **Repeat Inputs**

REVIEW: Change the data format to look at inputs AF through A8 in binary as well as hex by the following procedure:

Press [DATA FORMAT], [▽ SET], [▷] twice, [INSERT], [▷],

[BINARY B R], [ASCII A Q], [DEMUX F V HEX], [BINARY B R], [ASCII A Q], [LATCH E U OCTAL],

[BINARY B R], [ASCII A Q], [GLITCH D T DECIMAL], [BINARY B R], [ASCII A Q], [SAMPLE C S],

[BINARY B R], [ASCII A Q], [BINARY B R], [BINARY B R], [ASCII A Q], [ASCII A Q],

[BINARY B R], [ASCII A Q], [EBCDIC 9 P ECL], [BINARY B R], [ASCII A Q], [PAGE↑ 8 O TTL].

The new data format should now look like Figure 10-15. The same inputs may be viewed in more than one radix. In Figure 10-15, AF through A8 are displayed in both hex and binary.

Display the reformatted information.

Press [DATA]. See Figure 10-16 which shows the corresponding data display for the data format of Figure 10-15. The binary representation of each hex word is clearly seen.

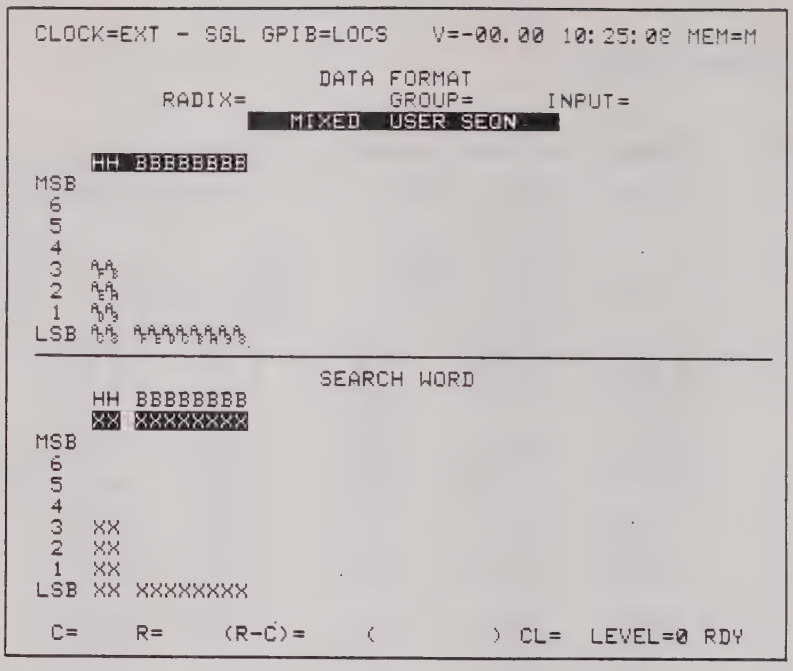


Figure 10-15. AF through A8 Displayed In Both Hex and Binary.

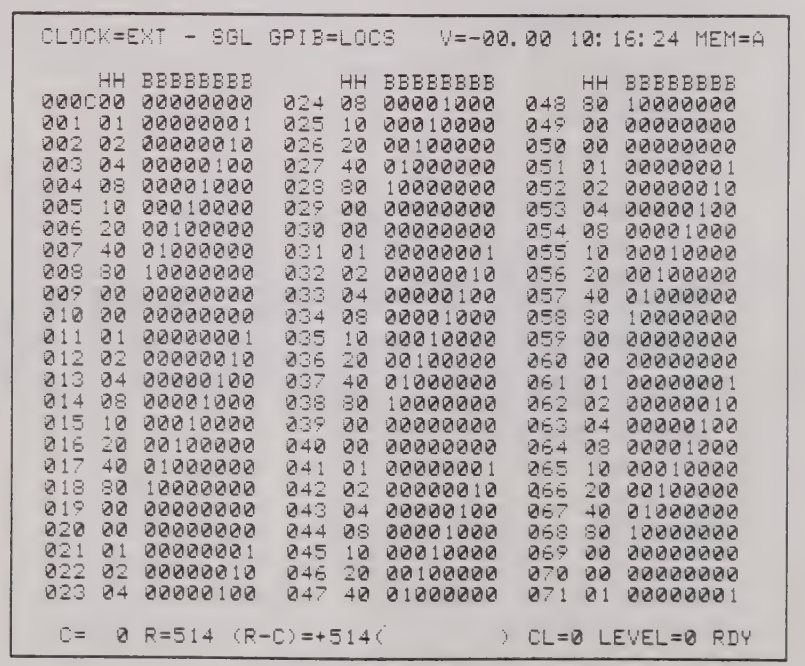


Figure 10-16. Data Display for Figure 10-15.

10.2.3.3 **Fixed Format**

REVIEW: Display the fixed binary format.

Press DATA FORMAT , Hx6 2 ' .

The display data should now look like Figure 10-17 which shows the same information viewed in a fixed binary format of all inputs CF through A0. Verify that only the first 14 binary columns (which are all zeros) are graphed.

Press GRAPH (see Figure 10-18) note that the graph of the first 14 columns of the fixed binary data display yields all zeros.

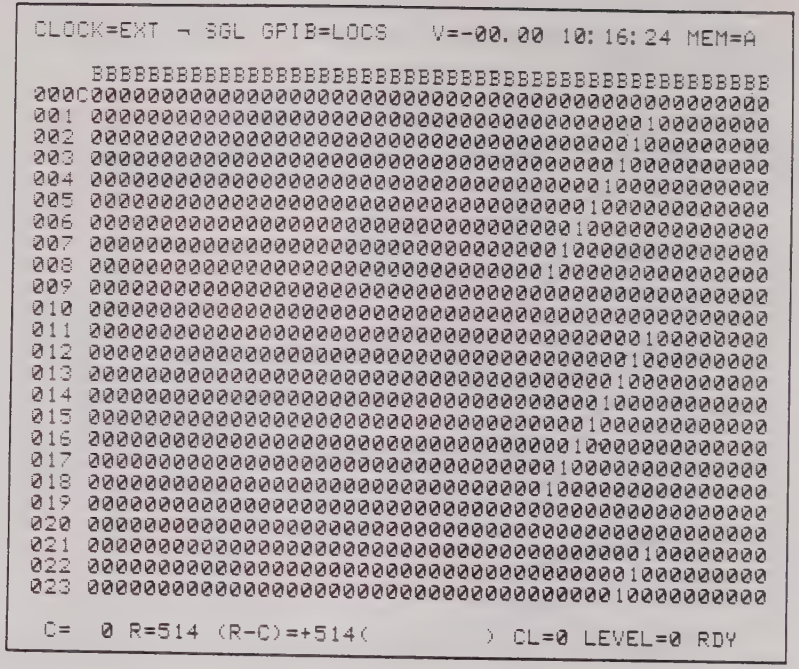


Figure 10-17. Fixed Binary Format, All Inputs CF through A0.

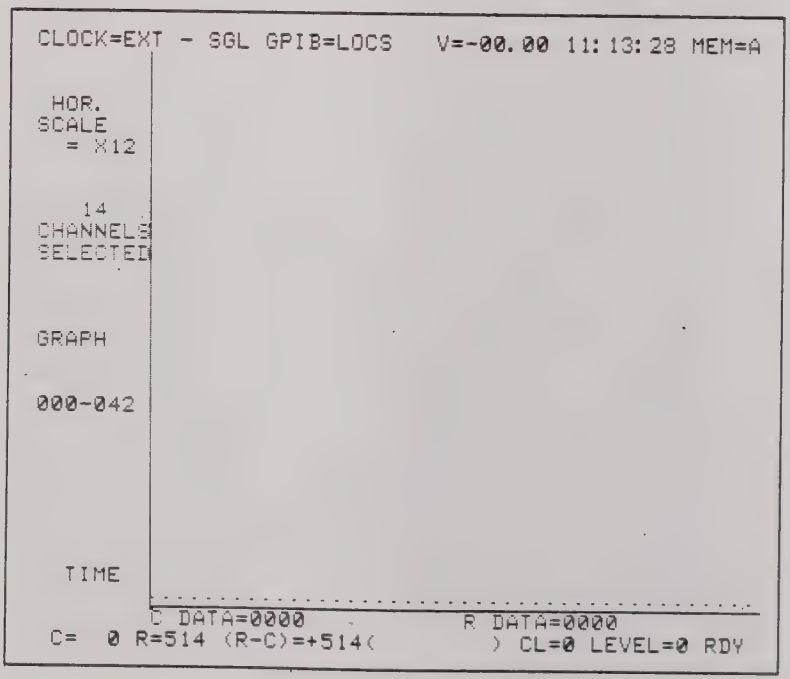


Figure 10-18. Graph First 14 Columns as Fixed Binary Data.

10.2.4 CLOCK AND INPUT

The Probe Test pattern generator produces two clock signals in addition to its eight data signals. The first clock signal is an external J clock input for the high order (F through 8) probe of each section, or an R enable input for the low order (7 through 0) probe of each section. The second clock signal is an external K clock input for the high order probe of each section, or an S enable input for the low order probe of each section. The actual time relationship between the clock and data signals is shown in Figure 10-19.

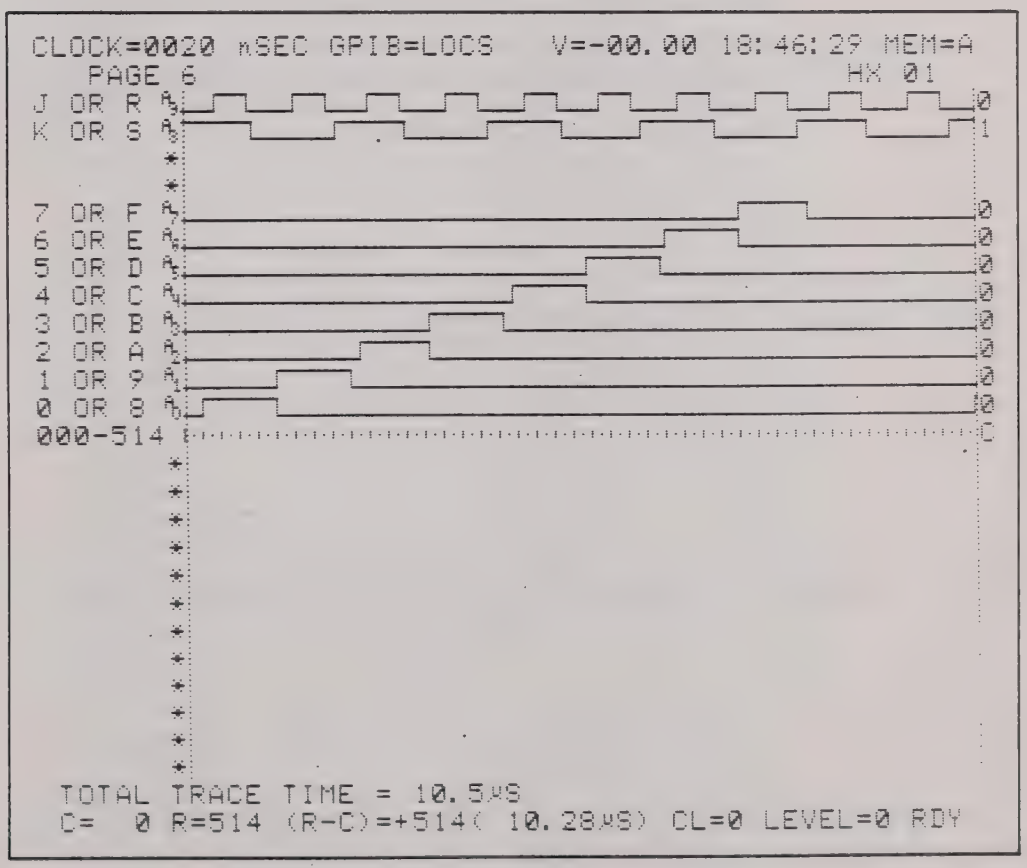


Figure 10-19. Time Relationship of Clock and Data Signals.

10.2.4.1 Sample Internally

SET UP: Take several samples of each pulse. See setup guide in Figure 10-20.

Modify Clock Select screen. Press [CLOCK SELECT], [Hx1 0 G], [▽ SET], [Hx3 1 H], [Hx1 0 G], [Hx1 0 G].

Display data format. Press [DATA FORMAT], [Hx12 3 J], [▽ SET], [▷] twice, [SHIFT], [DELETE].

The Clock Select and Data Format displays should look like Figures 10-21 and 10-22.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.1 OF ___ DATE _____

QUICK KEY (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
6	
D N 5	
A P 4	
T U 3	AcA8
A T 2	A6 A4
S 1	A2 A0
LSB	A6 A0

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count - Delay
4	If DATA = D and Sample Count - Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count - = Delay
7	If DATA = D and Sample Count - = Delay
8	If DATA = D and Sample Count - Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F) — COMMENTS

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = Q 1

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(____) STOP
S =

(____) JUMP TO ___ (O-F)
J =

(____) ADVANCE
A =

(____) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(____) STOP
S =

(____) JUMP TO ___ (O-F)
J =

(____) ADVANCE
A =

(____) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(____) STOP
S =

(____) JUMP TO ___ (O-F)
J =

(____) ADVANCE
A =

(____) TRACE
T =

Figure 10-20. Set Up Internal Sampling (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (..0..) MODE = INTERNAL

	CJ	BJ	AJ	CK	BK	AK
INTERNAL CLOCK PERIOD = 100				■ NANOSECONDS (20-1600) □ MICROSECONDS (1-1600) □ MILLISECONDS (1-160)		
MASTER = ■ INTERNAL □ EXT	(_____●_____●_____)			+ (_____+_____+_____)		
SECTION C = INT ■ SAME AS MASTER □ 10 NANOSECONDS						
EXT □ SAME AS MASTER □ (_____●_____●_____)				+ (_____+_____+_____)		
SECTION B = INT ■ SAME AS MASTER □ 10 NANOSECONDS						
EXT □ SAME AS MASTER □ (_____●_____●_____)				+ (_____+_____+_____)		
SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS						
EXT □ SAME AS MASTER □ (_____●_____●_____)				+ (_____+_____+_____)		

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS
SECTION C =	(_____●_____●_____)			+ (_____+_____+_____)		
SECTION B =	(_____●_____●_____)			+ (_____+_____+_____)		
SECTION A =	(_____●_____●_____)			+ (_____+_____+_____)		

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - A0 sequence.
1	OCTAL Fixed octal format & CF - A0 sequence.
2	BINARY Fixed binary format & CF - A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF - A0 SEQN Any radix, fixed CF - A0 sequence.
5	DEVICE MNEMONICS Fixed decompressed HP code format, only if RTE-816 emulator. OR
5	DEVICE NOT AVAILABLE No RTE-816 emulator.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate. Section A - Section B - Section C - Internal clock
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate. Section A - Section B - Section C - Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master external or internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C - Master external or internal or 10ns.
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and or Section C - Internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	_____	_____	_____
C7 — C0	_____	_____	_____
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	_____	_____	_____

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (..0..) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-612 R: 0-612

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-20. Set Up Internal Sampling (Sheet 2 of 2).

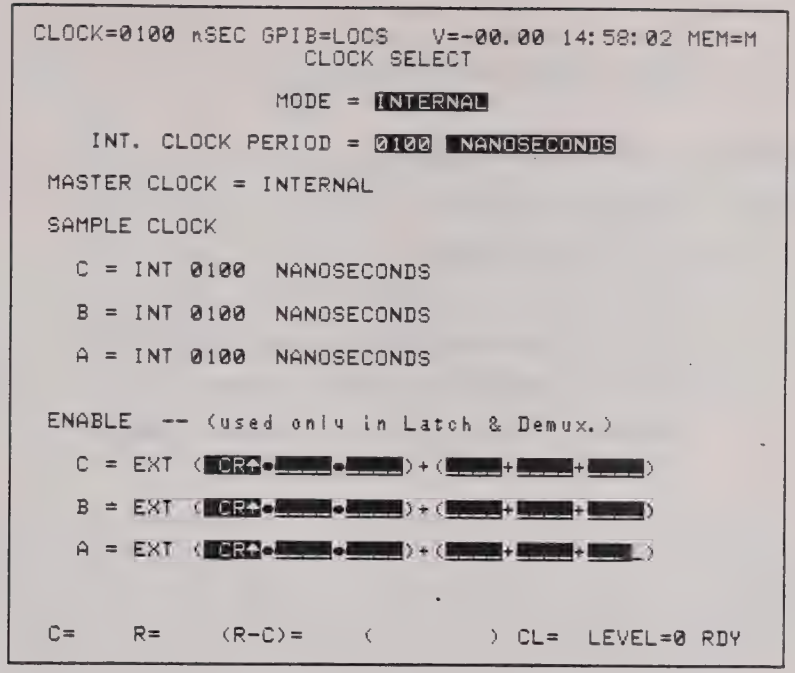

Figure 10-21. Clock Select for Sample Internally.

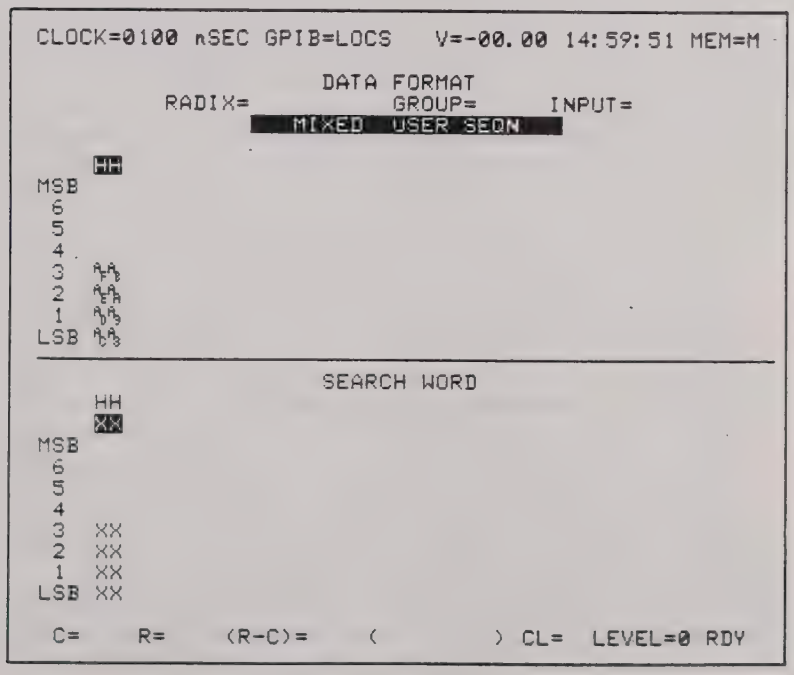

Figure 10-22. Data Format for Sample Internally.

RECORD: Press ARM .

REVIEW: Display the timing screen. Press TIMING , Hx1 0 G ,
PAGE 4 K to page 4.

The display should look like Figure 10-23. Each pulse is 0.9 microseconds (nine samples) wide ±100 nS (one sample). Confirm this with the cursors.

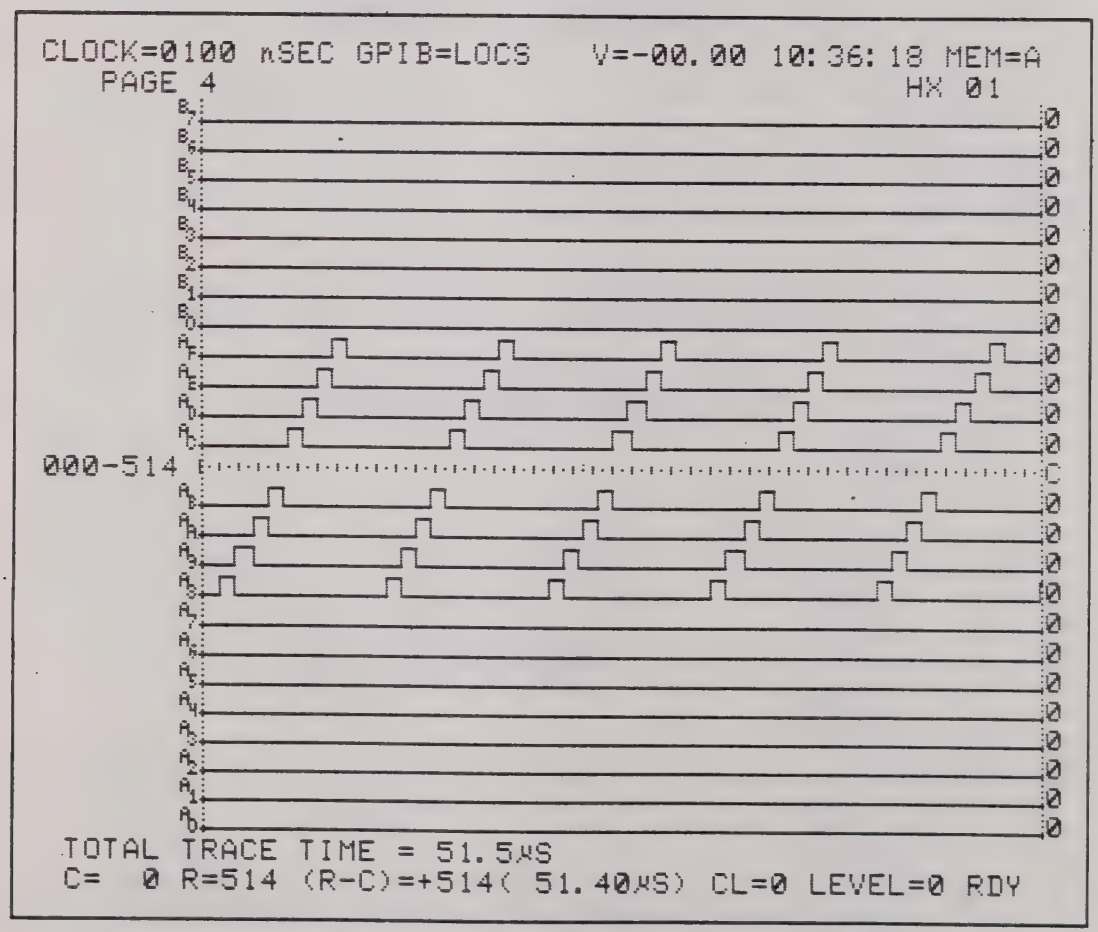

Figure 10-23. Pattern Asynchronously Sampled Every 100 ns.

10.2.4.2 **Sample On A Single External Clock (AJ↑ or AJ↓)**

SET UP: The active sampling edge of AJ can be specified as either rising or falling. Since both edges of each AJ pulse occur well within each input pulse (Figure 24a and 24b), it doesn't matter which edge is selected; the resulting recordings will be identical. In each case, one sample of each pulse will be taken. See the setup guide in Figure 10-25.

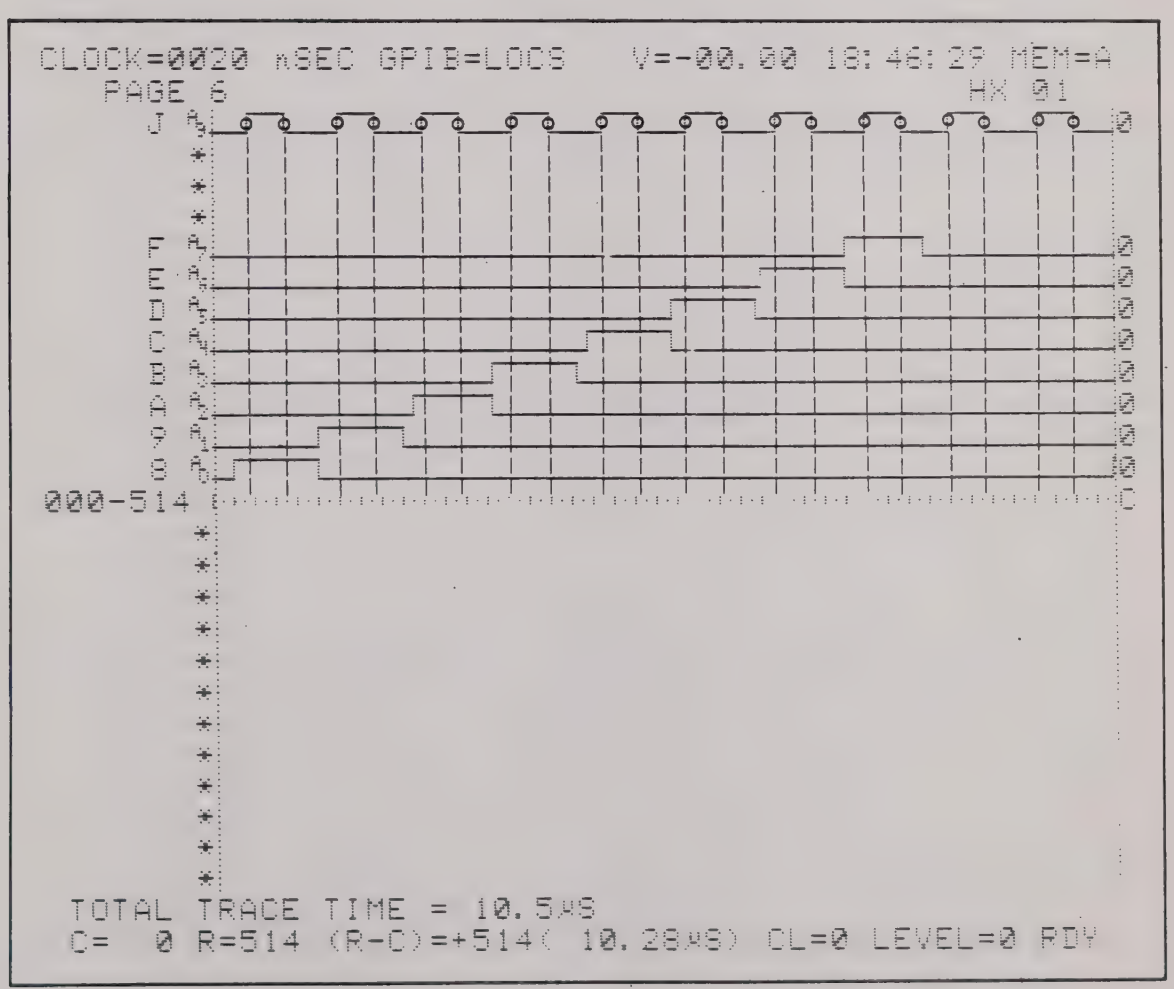

Figure 10-24. Sample Clock = AJ↑.

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ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #4.2 OF ___ DATE _____

QUICK KEY (See back for notes) (3.) DATA FORMAT MIXED USER SEQN.

RADIX: H H

	MSB	
	16	
DATA	15	
APT	14	
TU	13	A E A B
AT	12	A E A A
	11	A D A 9
	LSB	A C A 8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = 0
1	Always
2	Never
3	If DATA = D and Sample Count < Delay
4	If DATA = D and Sample Count = Delay
5	If DATA = D and Sample Count > Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA = D and Sample Count ≤ Delay
8	If DATA = D and Sample Count ≠ Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (Q-F) DELAY = DEC 515 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (Q-F) — COMMENTS

(3.) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY
S = 0 1

(2.) JUMP TO 0 (Q-F) NEVER
J = X X

(2.) ADVANCE NEVER
A = X X

(1.) TRACE ALWAYS
T = X X

LEVEL ___ (Q-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (Q-F) — COMMENTS

(___) STOP
S =

(___) JUMP TO ___ (Q-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

LEVEL ___ (Q-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (Q-F) — COMMENTS

(___) STOP
S =

(___) JUMP TO ___ (Q-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

LEVEL ___ (Q-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (Q-F) — COMMENTS

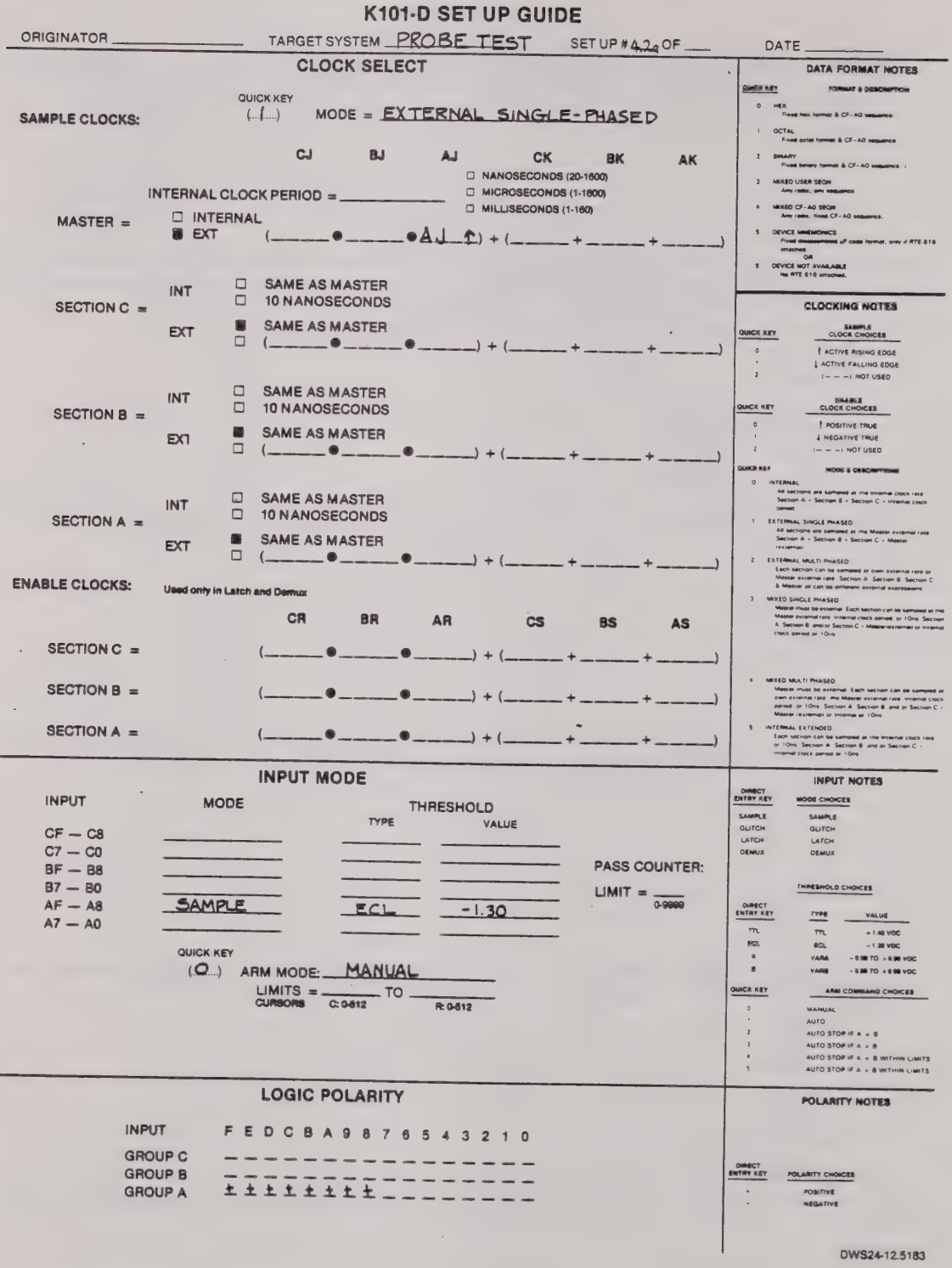
(___) STOP
S =

(___) JUMP TO ___ (Q-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

Figure 10-25. Setup Sample, Single External Clock (Sheet 1 of 2).



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ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.2a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (...f...) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↑) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence.
1	OCTAL — Fixed octal format & CF-A0 sequence.
2	BINARY — Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN — Any radix, any sequence.
4	MIXED CF-A0 SEQN — Any radix, Fixed CF-A0 sequence.
5	DEVICE MNEMONICS — Fixed disassembled uP code format, only if RTE-816 attached. OR
6	DEVICE NOT AVAILABLE — No RTE 816 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL — All sections are sampled at the internal clock rate. Section A + Section B + Section C + internal clock period
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A + Section B + Section C + Master (external)
2	EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external frequencies.
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C - Master as external or internal clock period or 10ns.
4	MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C - Master as external or internal or 10ns.
5	INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and/or Section C - internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	_____	_____	_____
C7 — C0	_____	_____	_____
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	_____	_____	_____

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (.Q...) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-612 R: 0-612

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
II	VARA	-5.00 TO +5.00 VDC
II	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-25. Setup Sample, Single External Clock (Sheet 2 of 2).

Change Clock Select display to show the following:

MASTER CLOCK = (__•__•__ AJ↑) + (__+__+__)

Press [CLOCK SELECT] , [Hx3 1 H] , [SET ▽] twice, [▷] twice, [Hx1 0 G] .

The Clock Select display should look like Figure 10-26 which shows clock select for setup AJ↑. Each subsequent push of [CLOCK SELECT] measures the external master sample clock frequency. . Note that if you press **CLOCK SELECT** a second time after setting it up, a reading of the external master clock frequency is displayed. Each press of **CLOCK SELECT** takes another frequency measurement.

RECORD: Press [ARM] .

REVIEW: Display the Timing screen.

Press [TIMING] , [Hx12 3 J] .

The display should look like Figure 10-27. Confirm that either active edge will create the same recording.

Press [A→B] , [CLOCK SELECT] , change active edges [SET ▽] twice, [▷] twice, [Hx3 1 H] , [ARM] , [DATA] , [COMPARE A/B] .

There should be no inequalities. Turn off the Comparison mode. Press [COMPARE A/B] .

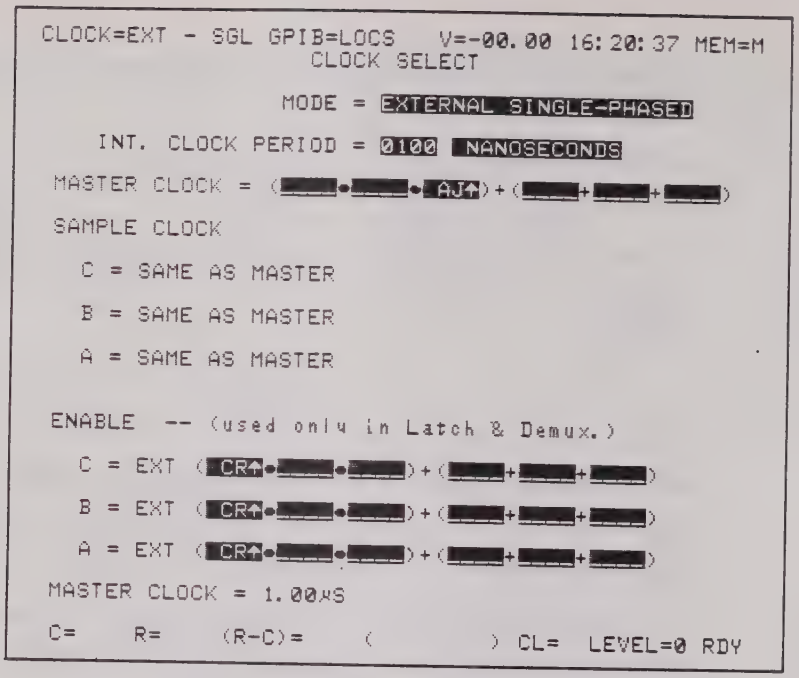

Figure 10-26. Clock Select for AJ↑.

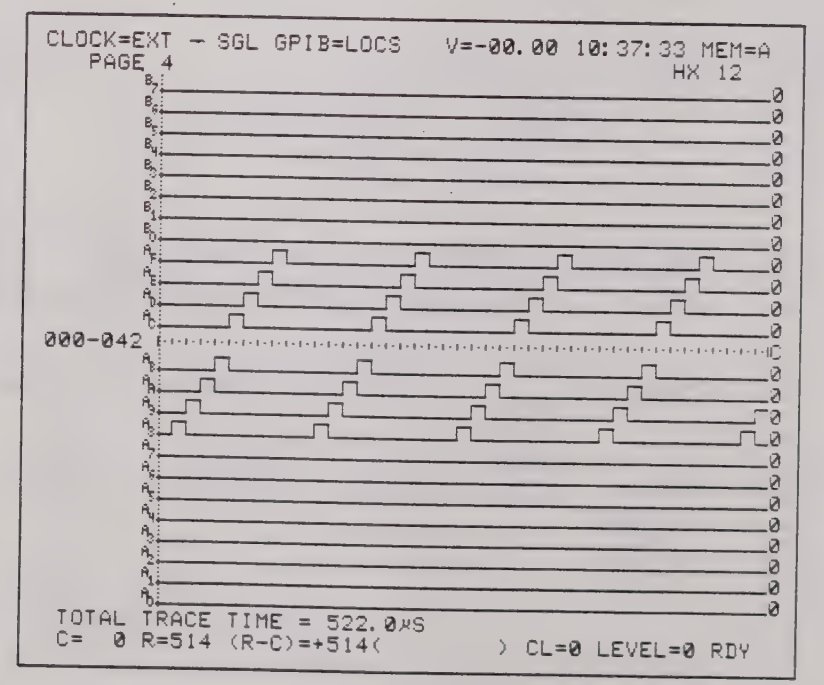

Figure 10-27. Recording for Sample Clock = AJ↑ or AJ↓.

10.2.4.3 **Sample on a Pair of External Clocks (AJ↓ and AK↑)**

SET UP: See setup guide in Figure 10-28.

A sample will be taken at each rising edge of the resultant sample clock which is created by combining AJ| and AK^ into a logical OR expression (Figure 10-29). Each odd-numbered input pulse is sampled once.

Change Clock Select display to the following:

MASTER CLOCK = (___·___· AJ↓) + (__ + __ + AK↑)

Change trace control to S = 02

Press [CLOCK SELECT], [▽] SET twice, [▷] twice, [1] Hx3 H,
[TRACE CONTROL], [▽] SET twice, [0] Hx1 G, [2] Hx6 F.

RECORD: Press [ARM].

REVIEW: Display timing screen. Press [TIMING].

The display should look like Figure 10-30. See Figures 10-31 and 10-32 for clocking with AJ↑ + AK↓. For Figure 10-31, a sample is taken at each rising edge of the resultant sample clock. Each even numbered input pulse is sampled twice. See Figures 10-33 and 10-34 for clocking with AJ↓ and AK↓. For Figure 10-33, a sample is taken at each rising edge of the resultant sample clock. Each even-numbered input pulse is sampled once.

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ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #4.3b OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AcAB
A T 2 AcAA
S 1 AcA9
LSB AcA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions.

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count - Delay
4	If DATA = D and Sample Count Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count - = Delay
7	If DATA = D and Sample Count - = Delay
8	If DATA = D and Sample Count - Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

QUICK KEY LEVEL 0 (0-F) DELAY = DEC 515 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

COMMENTS

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 2

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

QUICK KEY LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

COMMENTS

(___) STOP _____
S = _____

(___) JUMP TO ___ (0-F) _____
J = _____

(___) ADVANCE _____
A = _____

(___) TRACE _____
T = _____

QUICK KEY LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

COMMENTS

(___) STOP _____
S = _____

(___) JUMP TO ___ (0-F) _____
J = _____

(___) ADVANCE _____
A = _____

(___) TRACE _____
T = _____

QUICK KEY LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

COMMENTS

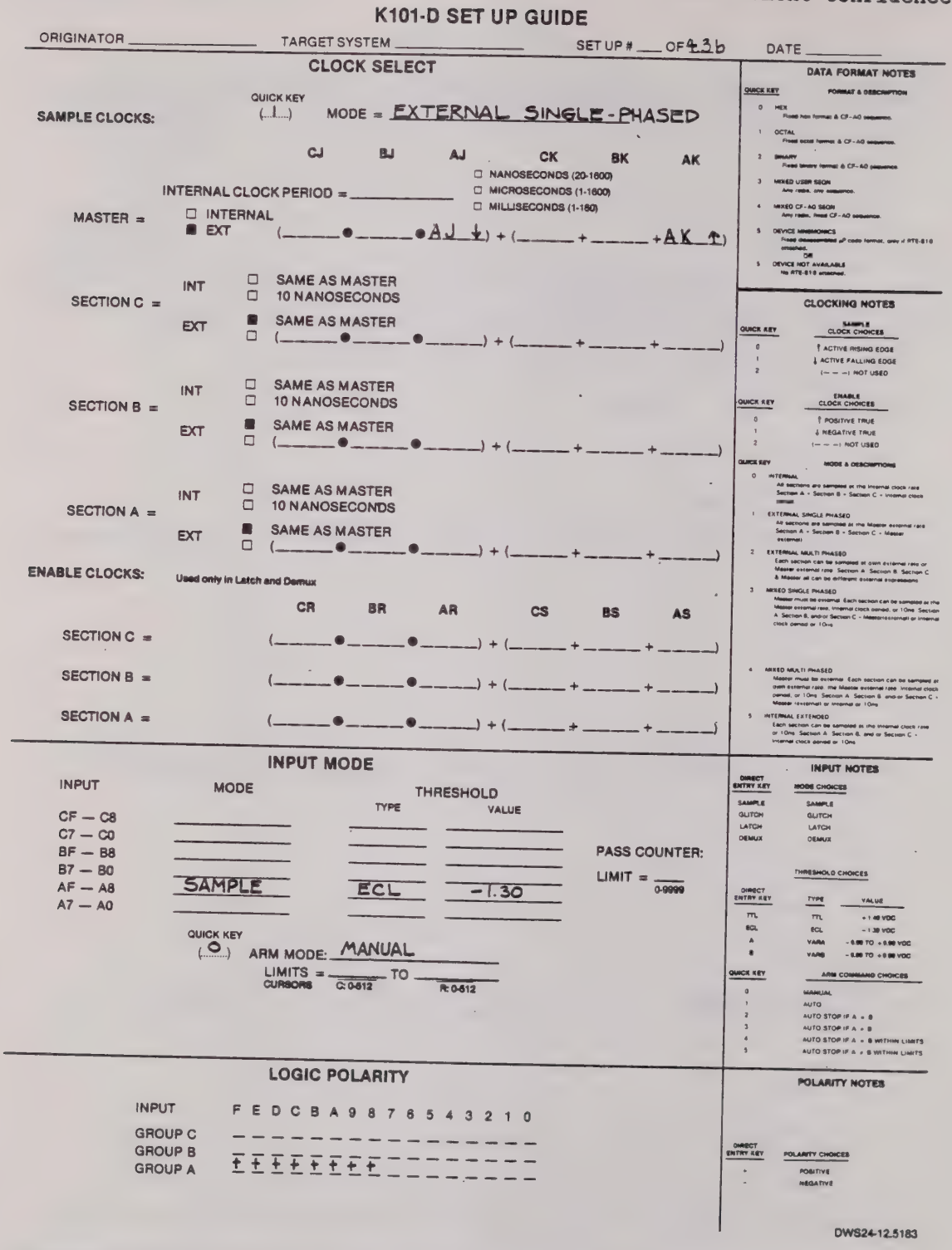
(___) STOP _____
S = _____

(___) JUMP TO ___ (0-F) _____
J = _____

(___) ADVANCE _____
A = _____

(___) TRACE _____
T = _____

Figure 10-28. Setup Guide Sample on Pair of External Clocks (Sheet 1 of 2).



K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF 43b DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+AK ↑)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed decode/printout of code format, only if RTE-810 attached. OR DEVICE NOT AVAILABLE no RTE-810 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate. Section A • Section B • Section C • Internal clock period

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate. Section A • Section B • Section C • Master (external)

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external signal sources.

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (external) or Internal clock period or 10ns

4 MIXED MULTI PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (external) or Internal or 10ns

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and or Section C - Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = CURSORS ____ (C: 0-512) TO ____ (R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	+	+	+	+	+	+	+	+	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-28. Setup Guide Sample on Pair of External Clocks (Sheet 2 of 2).

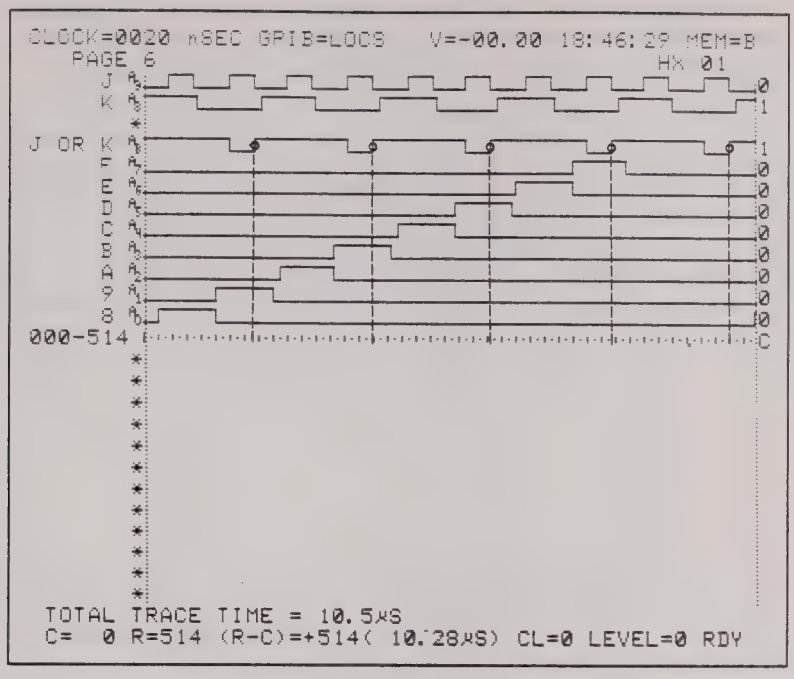


Figure 10-29. Sample Clock = AJ↓ + AK↑.

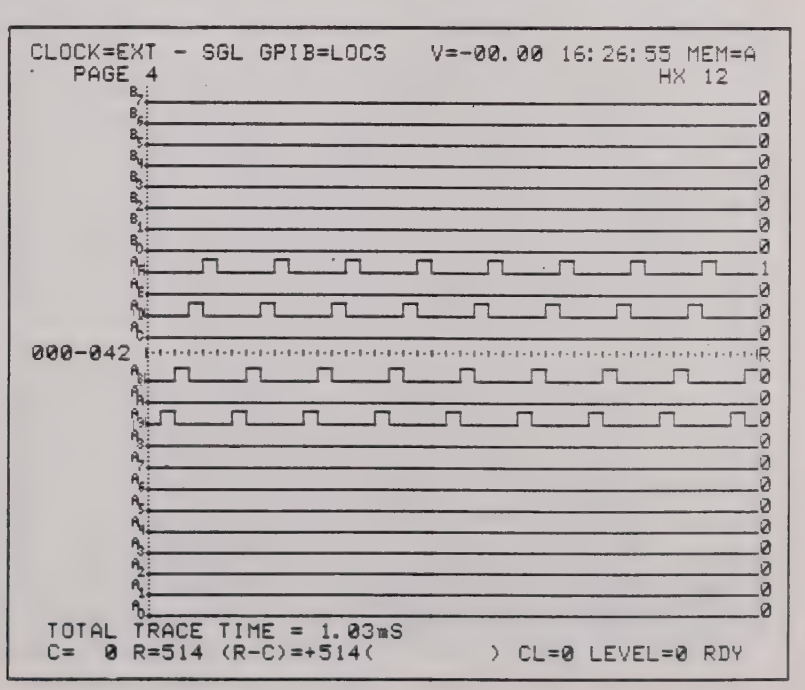


Figure 10-30. Recording for Sample Clock = AJ↓ + AK↑.

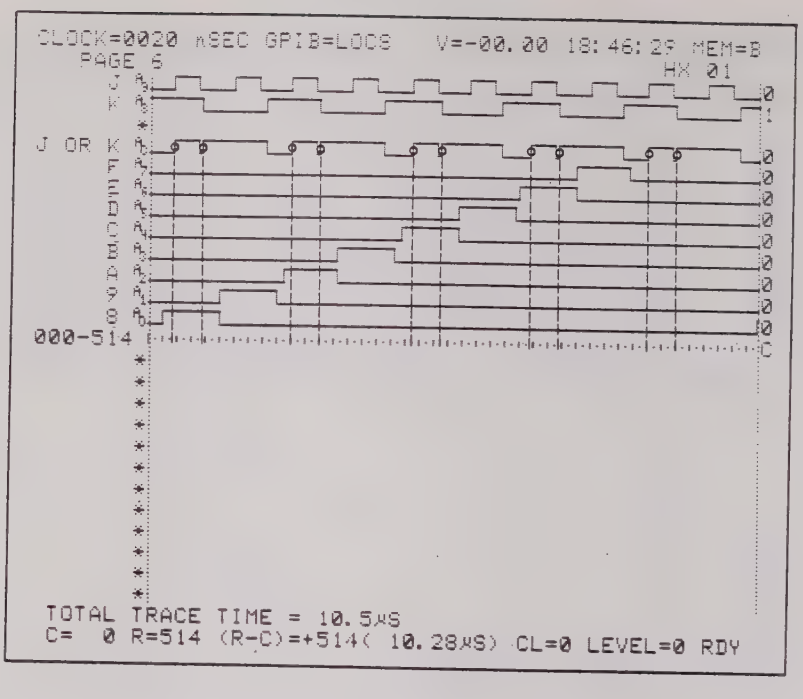


Figure 10-31. Sample Clock = AJ↑ + AK↓.

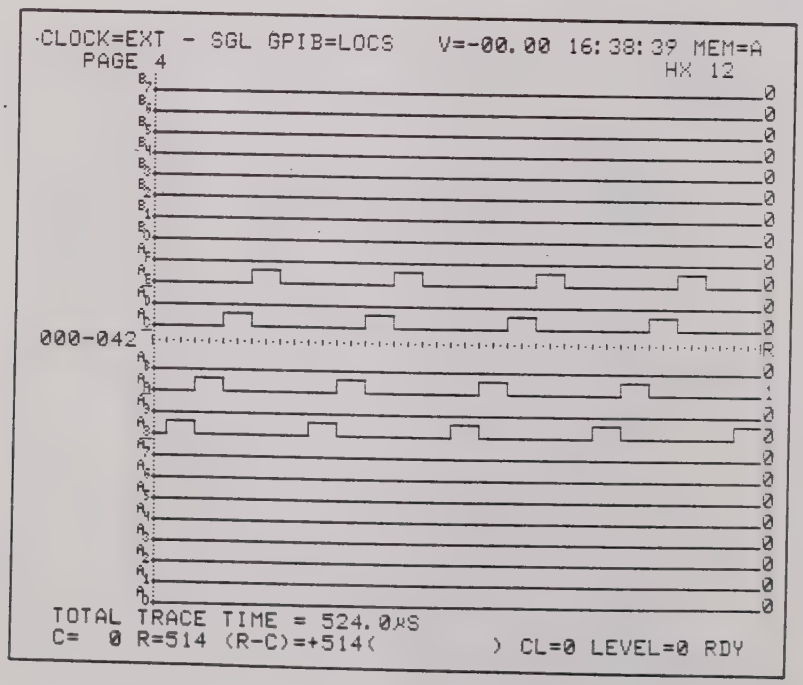


Figure 10-32. Recording for Sample Clock = AJ↑ + AK↓.

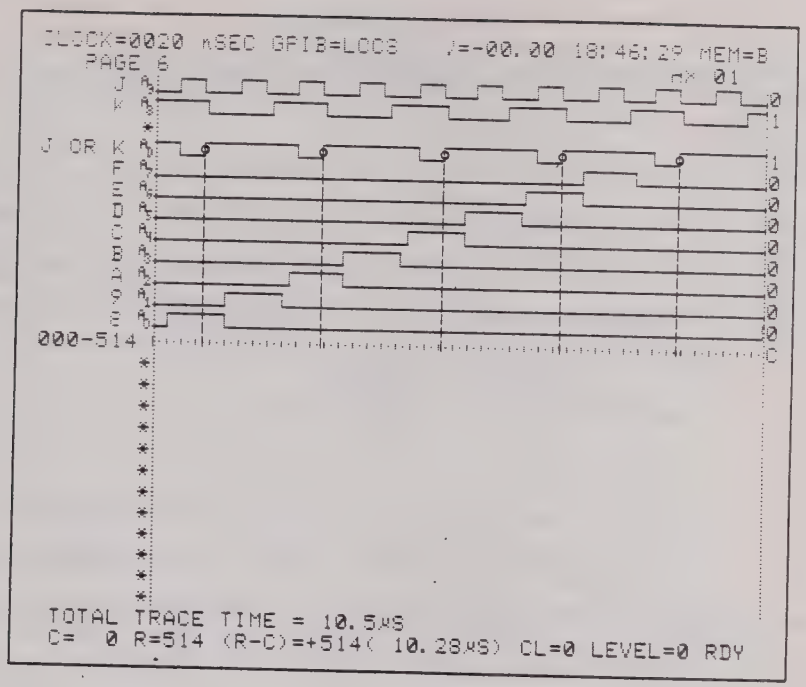


Figure 10-33. Sample Clock = AJ↓ + AK↓.

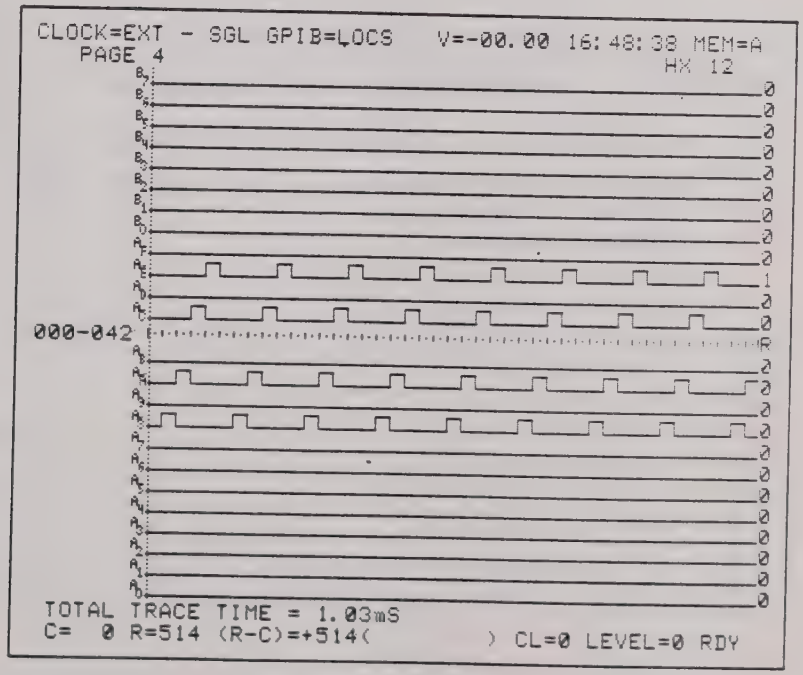


Figure 10-34. Recording for Sample Clock = AJ↓ + AK↓.

10.2.4.4 Latch (Enable) on a Single Input (AR↑, AR↓)

SET UP: See setup guide in Figure 10-35. Disconnect the AF through A8 probe from PROBE TEST connector and connect the A7 through A0 probe. Display page 6 of the Timing screen.

Press TIMING , PAGE 4 twice.

Inputs are held at the levels that exist when the latch enable signal goes false, then are released to be able to change when the signal is true. All transitions occur while the inputs are latched and, therefore, change synchronously with AR↑ going high. The latched inputs are then asynchronously sampled.

The inputs are latched while AR↑ is false (low) and released while it is true (high). Every transition is latched; therefore, all the inputs change synchronously with the rising edge of AR↑ (see Figure 10-36).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 44a OF ___ DATE _____

QUICK KEY (See back for notes) (..3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 A_1A_2
A T 2 A_4A_3
S 1 A_3A_1
LSB A_4A_0

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four mnemonic commands in each level can come true on any of nine conditions:

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA = D and Sample Count ≤ Delay
8	If DATA = D and Sample Count ≠ Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

QUICK KEY LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

COMMENTS

(..3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(..2) JUMP TO 0 (O-F) NEVER
J = X X

(..2) ADVANCE NEVER
A = X X

(..1) TRACE ALWAYS
T = X X

QUICK KEY LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

QUICK KEY LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

QUICK KEY LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

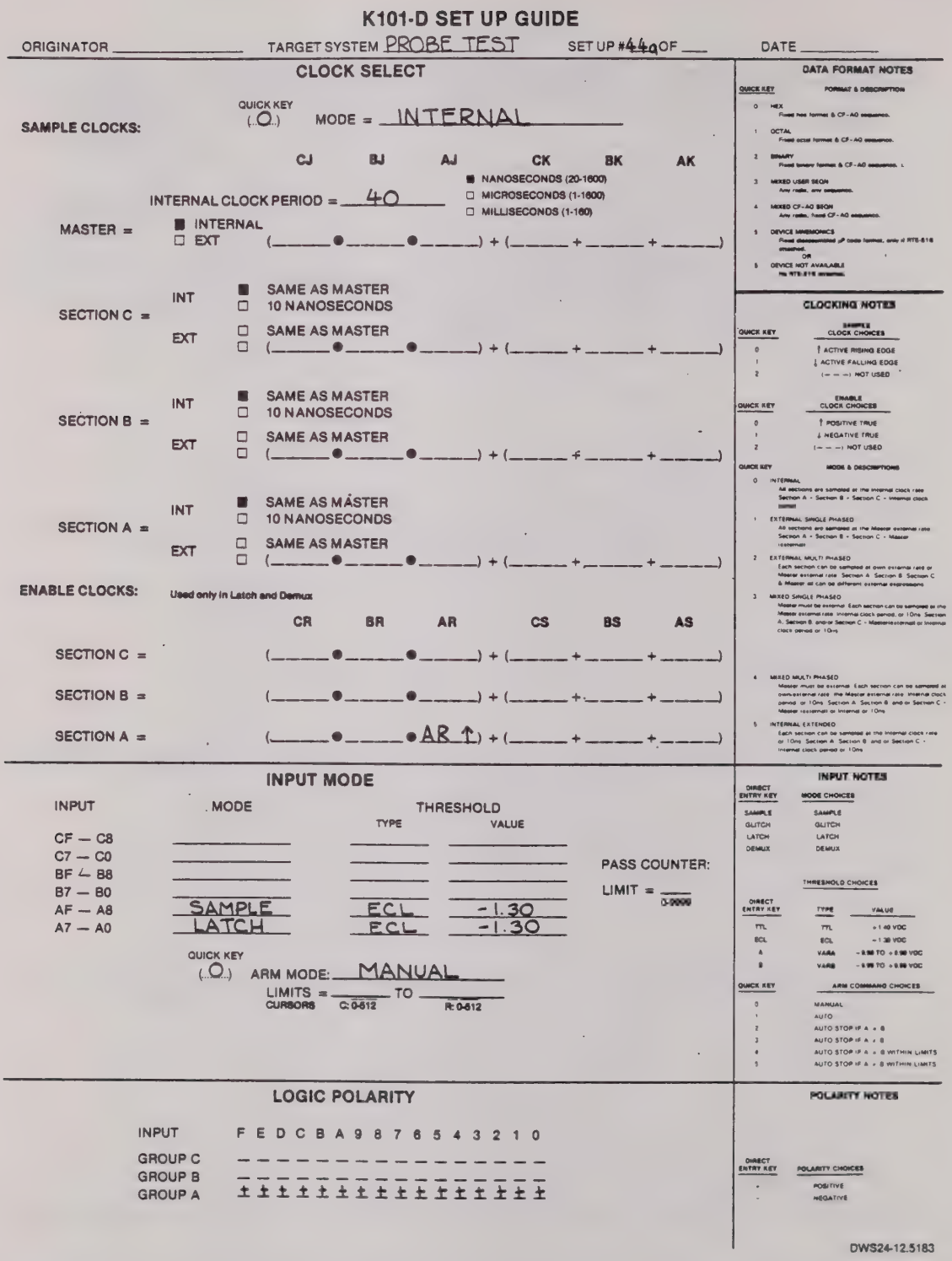
(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

Figure 10-35. Setup Latch (Enable) on a Single Input (Sheet 1 of 2).



K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #44a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (O) MODE = INTERNAL

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = 40

■ NANOSECONDS (20-1600)
□ MICROSECONDS (1-1600)
□ MILLISECONDS (1-160)

MASTER = ■ INTERNAL □ EXT (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION C = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____ ● _____ ● _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = (_____ ● _____ ● AR ↑) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed [illegible] μP code format, only if RTE-516 attached. OR
6	DEVICE NOT AVAILABLE No RTE-516 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate Section A Section B Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external Each section can be sampled at the Master external rate Internal clock period, or 10ns Section A, Section B and/or Section C - Master(external) or Internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external Each section can be sampled at own external rate the Master external rate Internal clock period or 10ns Section A Section B and or Section C - Master (external) or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns Section A Section B and or Section C - Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	LATCH	ECL	-1.30

PASS COUNTER:
LIMIT = ____ 0-9999

QUICK KEY (O) ARM MODE: MANUAL
LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	±	±	±	±	±	±	±	±

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-35. Setup Latch (Enable) on a Single Input (Sheet 2 of 2).

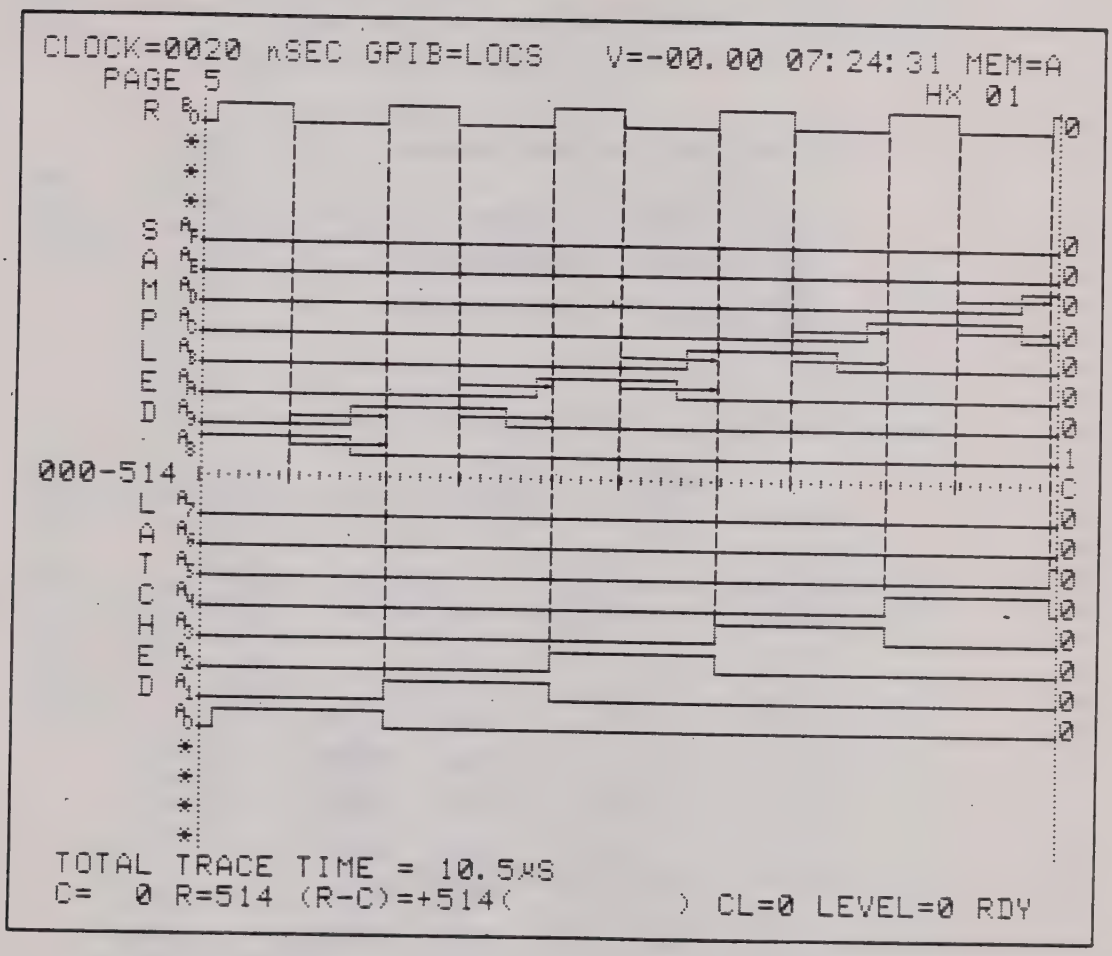


Figure 10-36. Enable = AR↑.

Set up the Clock Select screen.

Press [CLOCK SELECT] , [Hx1 0 G] , [▽ SET] , [PAGE ↓ 4 K] , [Hx1 0 G] , [▽ SET] three times, [Hx6 2 I] , [▷] twice, [Hx1 0 G] .

Display the Input Mode screen.

Press [INPUT MODE] , [△] twice, [LATCH E U OCTAL] , [▷] , [EBCDIC 9 P ECL] .

Display the Data Format screen.

Press [DATA FORMAT] , [▽ SET] twice, [ASCII A Q A] , [V6 7 N] , [ASCII A Q A] , [V12 6 M] , [ASCII A Q A] , [V24 5 L] , [ASCII A Q A] , [PAGE ↓ 4 K] , [▽ SET] , [ASCII A Q A] , [Hx12 3 J] , [ASCII A Q A] , [Hx6 2 I] , [ASCII A Q A] , [Hx3 1 H] , [ASCII A Q A] , [Hx1 0 G] .

Display Trace Control screen.

Press [TRACE CONTROL] , [▽ SET] twice, [Hx1 0 G] , [Hx3 1 H] .

Clock Select and Input Mode screens should look like Figures 10-37 and 10-38.

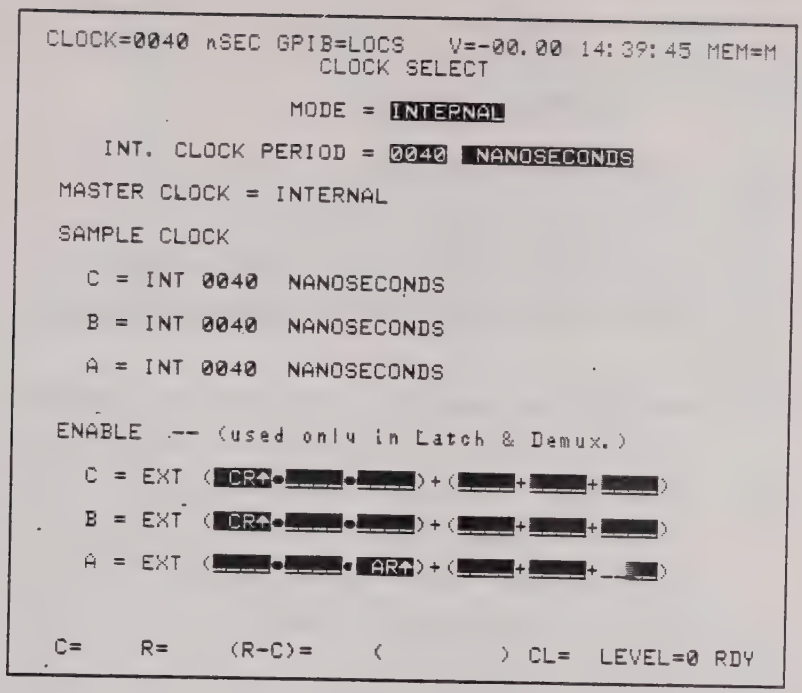


Figure 10-37. Clock Select for Enable = AR↑.

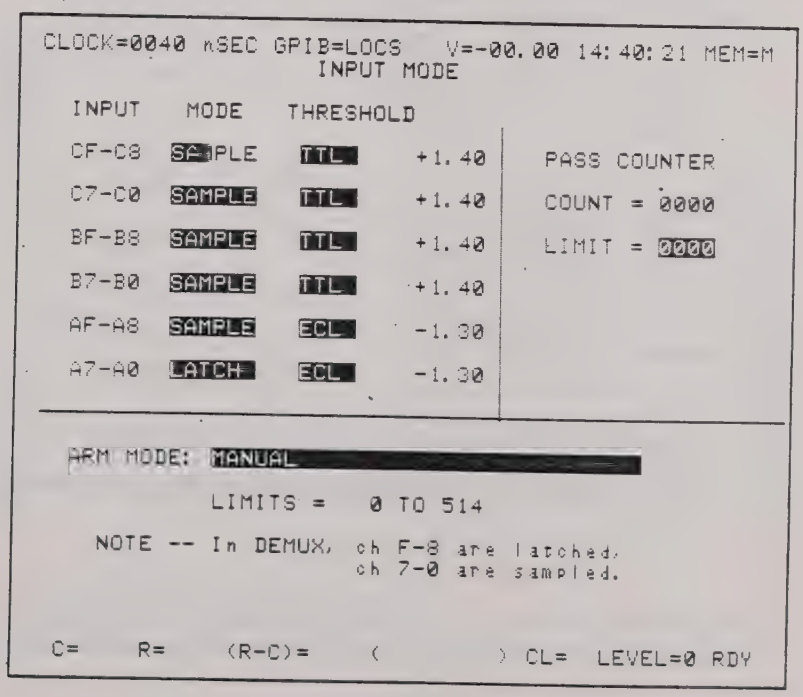


Figure 10-38. Input Mode for Latch on Single Input.

RECORD: Press ARM .

REVIEW: Display the Timing screen. Press TIMING .

The display should look like Figure 10-39. Note that all transitions now occur synchronously.

SET UP: When AR↓ is used, the inputs are latched while AR↓ is false (high) and released while it is true (low). Since the latching occurs totally within each pulse (i.e., no input signal transitions occur during the latch period), the latch signal has no effect on the inputs (see Figure 10-40).

Change the Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+__)

Press CLOCK SELECT , ▽ SET four times, ▷ twice, 1 Hx3 H .

RECORD: Press ARM .

REVIEW: Press TIMING .

When AR↓ is used this display should look like Figure 10-41. Note that the transitions are asynchronous.

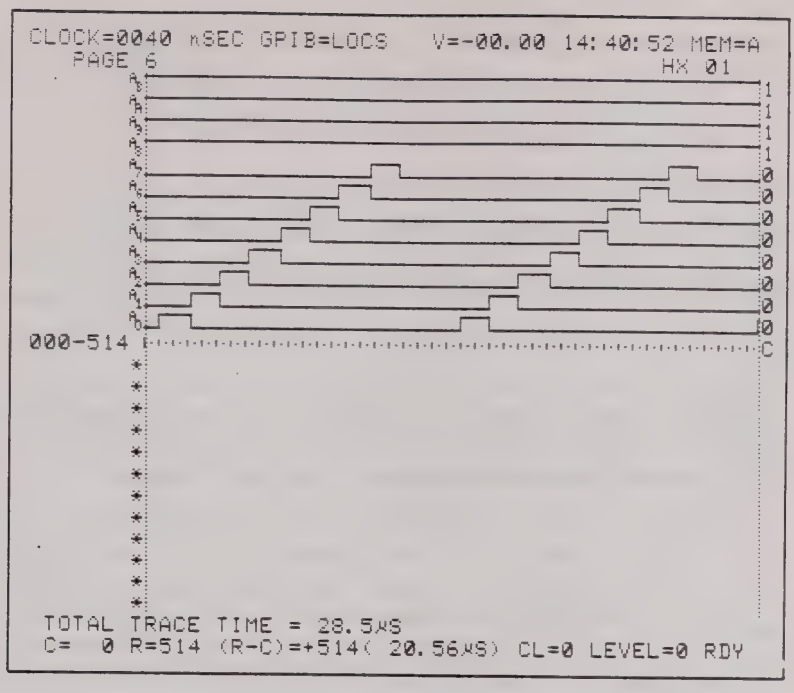


Figure 10-39. Recording of Asynchronously Sampled Latched Inputs for Enable = AR↑.

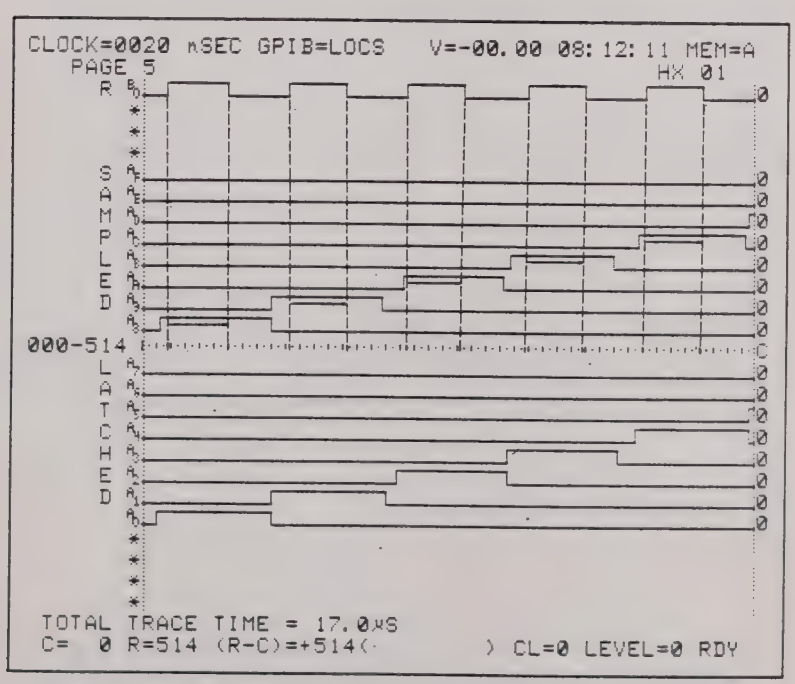


Figure 10-40. Function of Input Signal Transitions Latch Enable Signal.

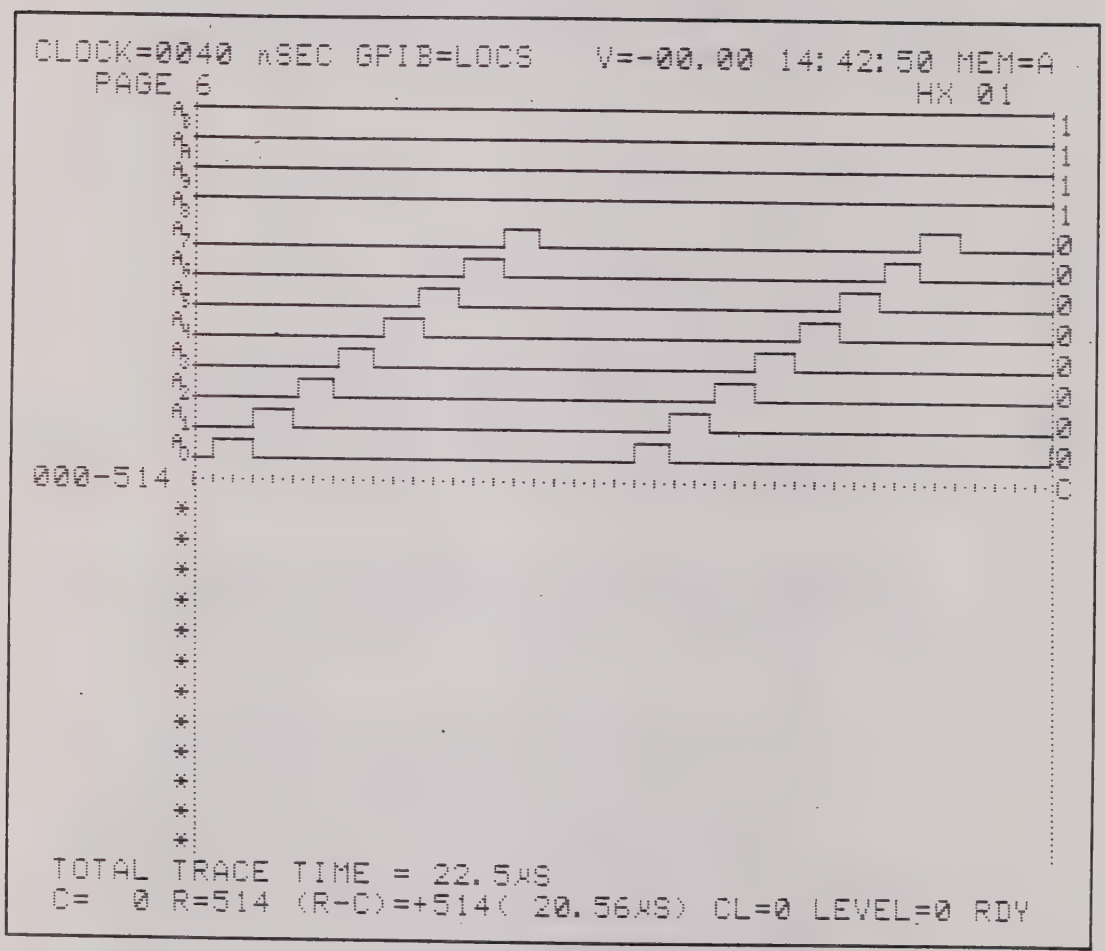


Figure 10-41. Recording for Enable = AR↓.

SET UP: When AS↑ is used the inputs are latched while AS↑ is false (low) and released while it is true (high). Every other transition is latched (see Figure 10-42). Note that every other input transition occurs during a latched period and, therefore, cannot change until enable returns to true.

When AS↑ is used the Timing display should look like Figure 10-43. Note that every other transition is synchronous.

SET UP: When AS↓ is used the inputs are latched while AS↓ is false (high) and released while it is true (low). Every other transition is latched (see Figure 10-44) or every other input transition AS↓ occurs during a latched period and, therefore, cannot change until enable returns to true.

When AS↓ is used the Timing display should look like Figure 10-45.

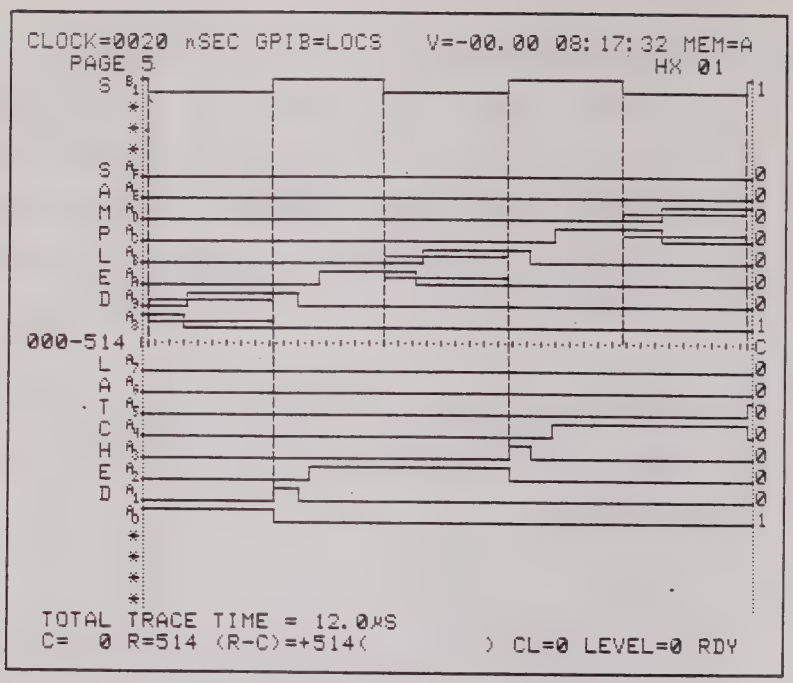


Figure 10-42. Enable = AS↑ Every Other Transition Latched.

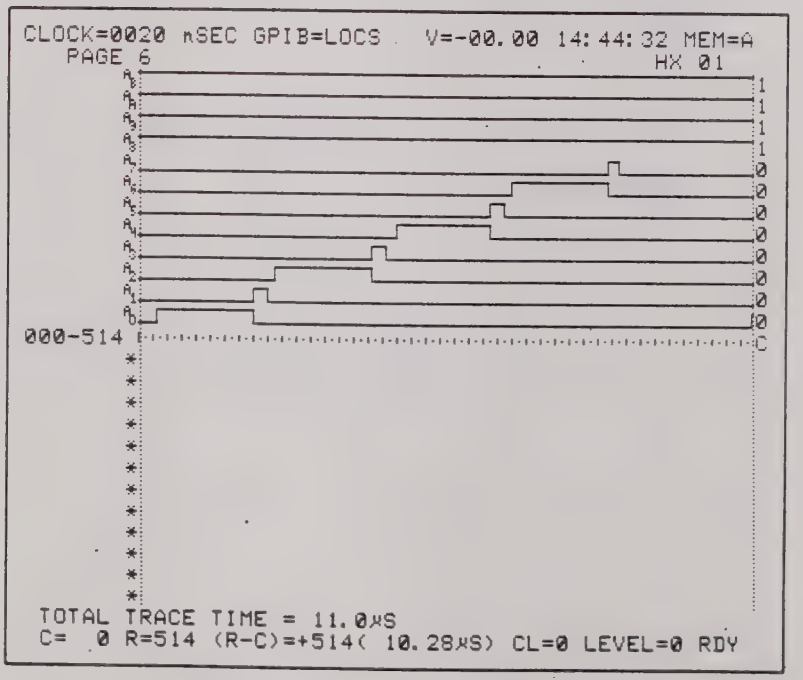


Figure 10-43. Time Recording for Enable = AS↑.

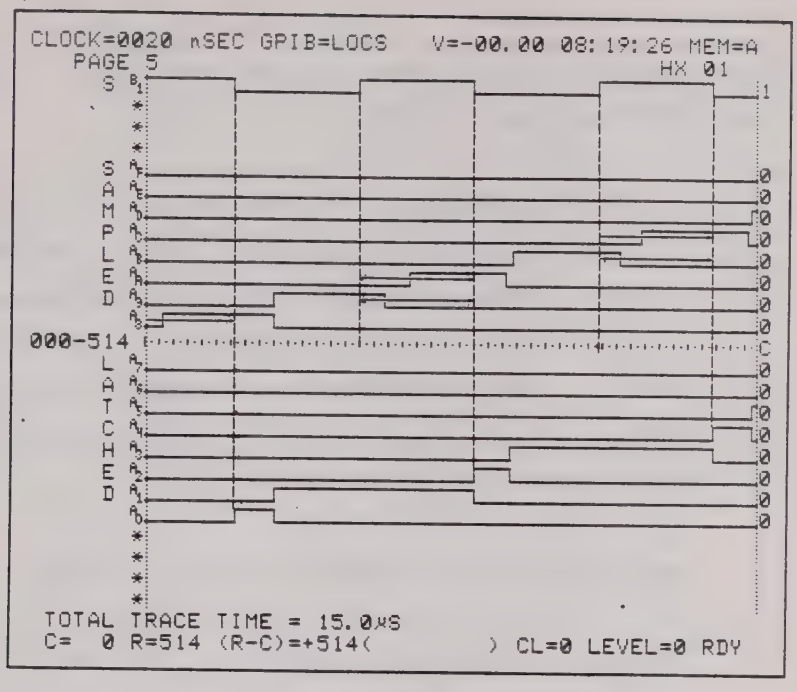


Figure 10-44. Enable = AS↓, Inputs Latched When AS↓ True.

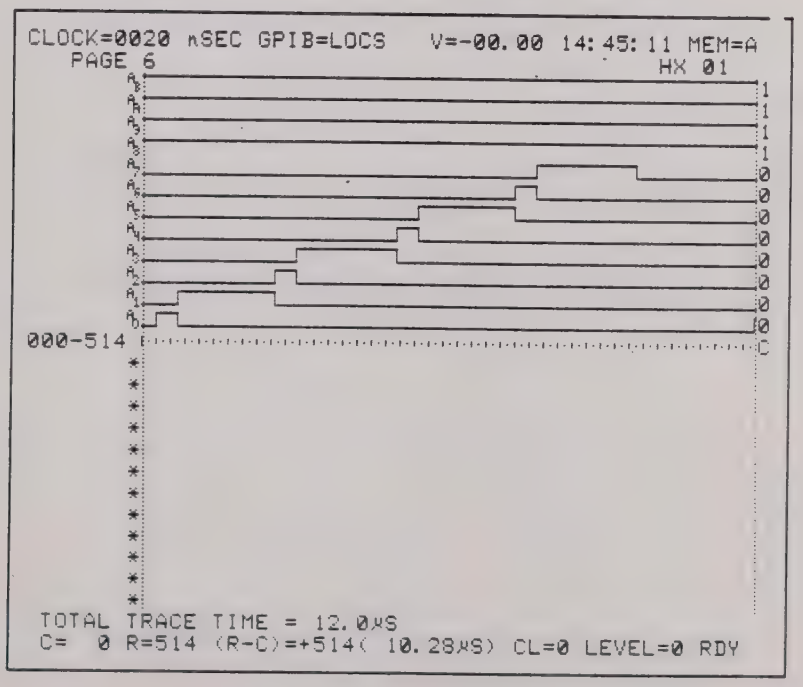


Figure 10-45. Recording for Enable = AS↓.

10.2.4.5 Latch (Enable) on a Combination of Inputs (AR↑ + AS↑, AR↓ + AS↑, AR↑ + AJ↓, AR↓ + AJ↓)

SET UP: The latch enable signal is created by combining AR^ and AS| into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Every other transition is latched (see Figure 10-46). Every other input transition occurs during a latched period and, therefore, cannot change until the enable expression becomes true.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↑) + (__+__+ AS↑)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx↑ 0 G], [▷] three times, [Hx↑ 0 G].

RECORD: Press [ARM].

REVIEW: Display the Timing screen. Press [TIMING].

The display should look like Figure 10-47.

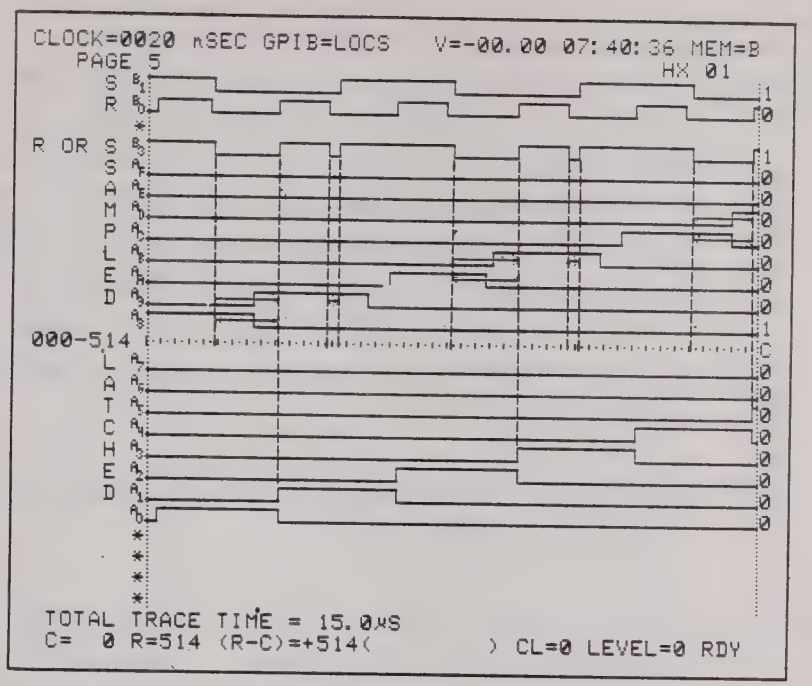


Figure 10-46. Enable = AR↑ + AS↑.

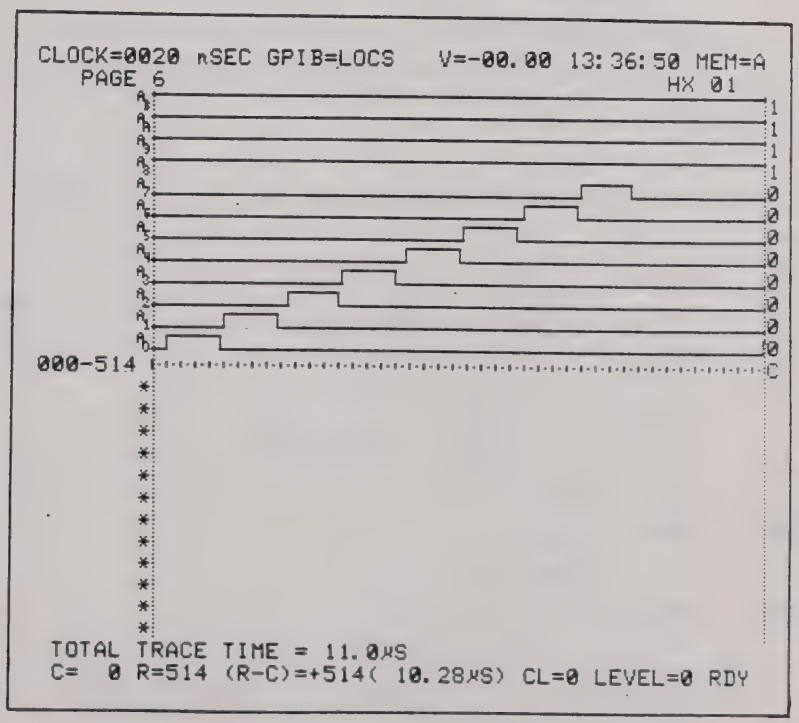


Figure 10-47. Recording for Enable = AR↑ + AS↑.

SET UP: When AR↓ + AS↑ is used, the latch enable signal is created by combining AR↓ and AS↓ into a logical OR expression. The inputs are latched while the resultant enable signal is false and released while it is true. Since latching occurs totally within every other pulse, the latch signal has no affect on the inputs (see Figure 10-48). No input transitions occur during a latched period; therefore, the Enable expression has no affect on the inputs.

When AR↓ + AS↑ is used, the Timing display should look like Figure 10-49.

SET UP: When AR↑ + AS↓ is used the latch enable signal is created by combining AR↑ and AS↓ into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Latching occurs at every other transition (see Figure 10-50). Note that every other input transition occurs during a latched period and, therefore, cannot change until enable becomes true.

Change Clock Select display to the following:

ENABLE A = EXT (__ • __ • AR↑) + (__ + __ + AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [0 G], [▷] three times, [1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↑ + AS↓ is used, the Timing display should look like Figure 10-51.

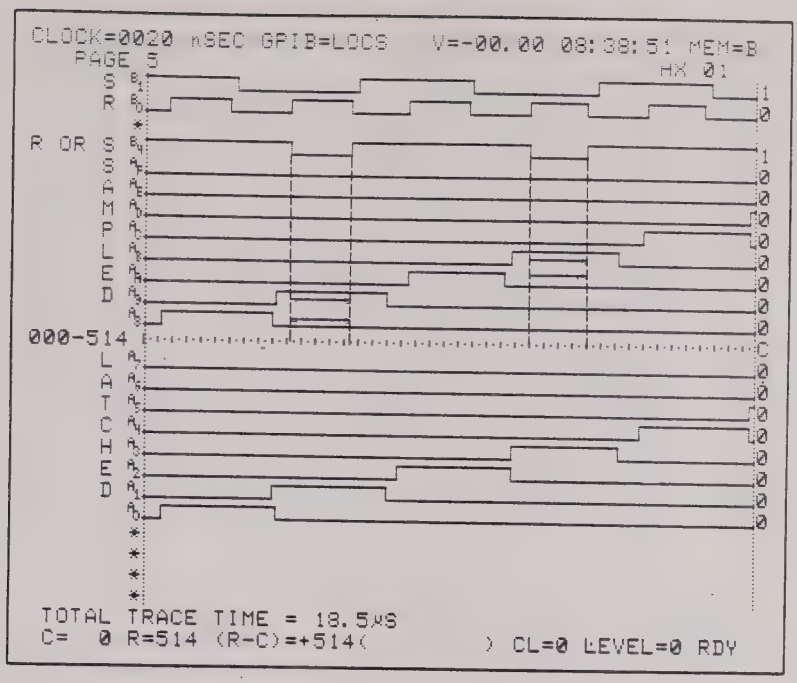


Figure 10-48. Enable = AR↓ + AJ↑.

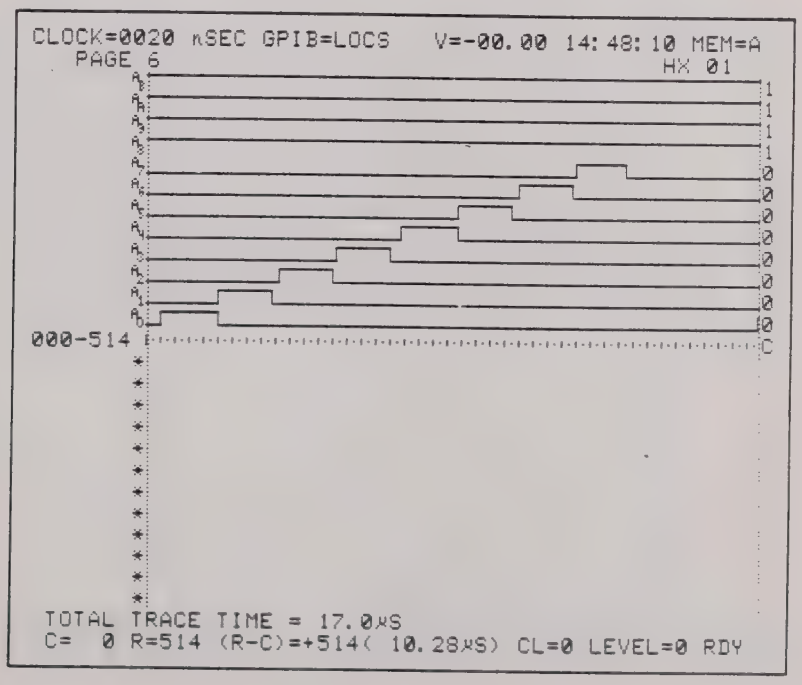


Figure 10-49. Recording for Enable = AR↓ + AS↑.

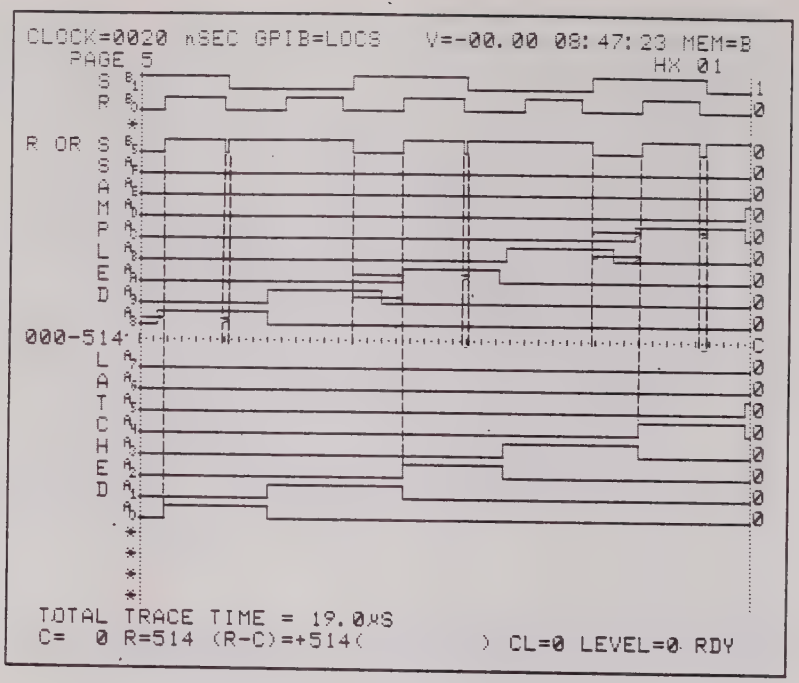


Figure 10-50. Enable = AR↑ + AS↓.

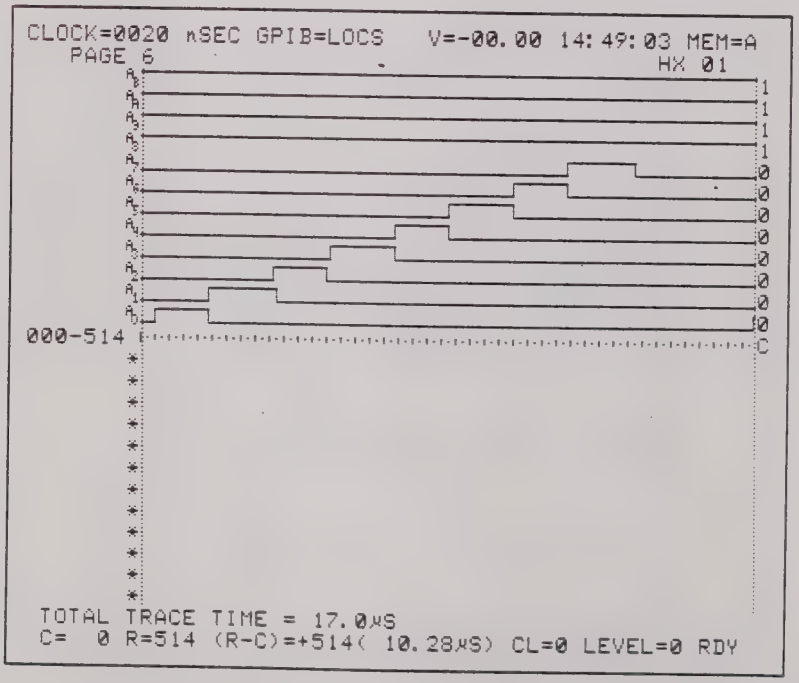


Figure 10-51. Recording for Enable = AR↑ + AS↓.

SET UP: When AR↓ + AS↓ is used the latch enable signal is created by combining AR↓ and AS↓ into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Since the latching occurs totally within every other pulse, the latch signal has no affect on the inputs (see Figure 10-52). Note that no input transitions occur during a latched period; therefore, latch enable has no affect on the inputs.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+ AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] five times, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↓ + AS↓ is used, the Timing display should look like Figure 10-53.

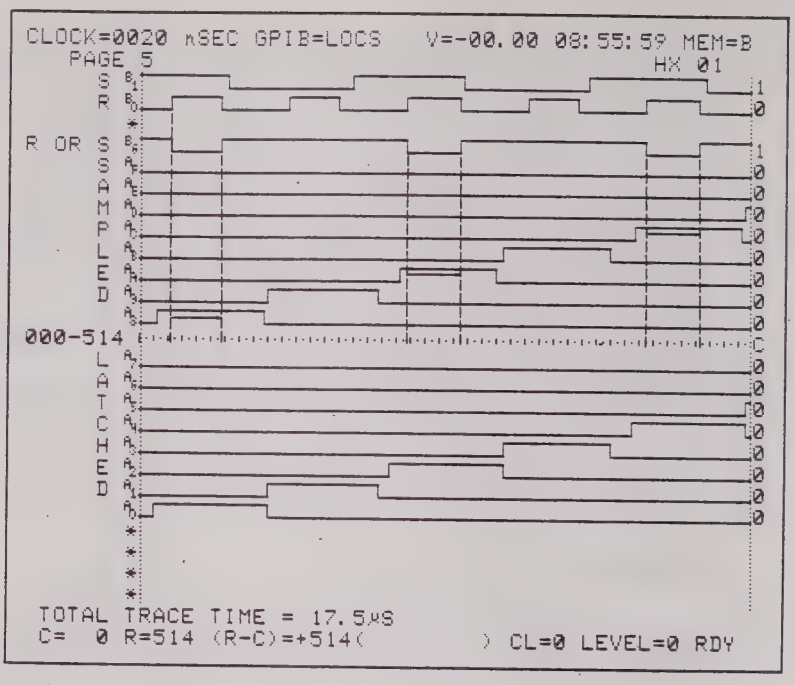


Figure 10-52. Enable = AR↓ + AS↓.

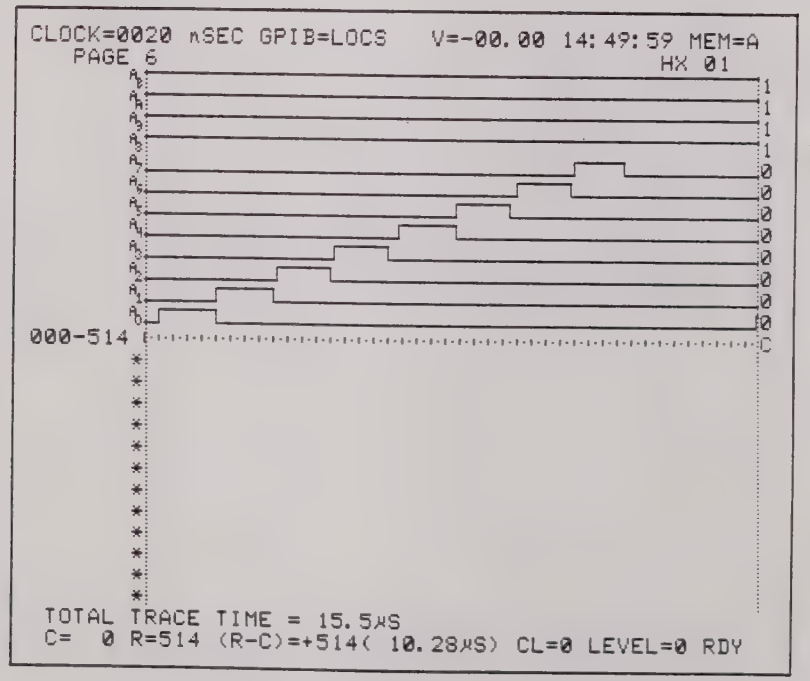


Figure 10-53. Recording for Enable = AR↓ + AS↓.

10.2.4.6 Demultiplex on a Single Enable Input (AR↑, AR↓, AS↑, AS↓)

SET UP: The inputs on A7 through A0 are put in the Sample input mode. The inputs on A7 to A0 are also sent to AF through A8 and latched there by the enable signal AR↑.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↑) + (__+__+__)

Change Input mode for inputs AF through A8 and A7 through A0 to display DEMUX.

Display Clock Select screen. Press [CLOCK SELECT], [+ ▽ SET] four times, [+ ▷] twice, [Hx1 0 G], [+ ▷] three times, [Hx6 2 I].

Display Input Mode screen. Press [INPUT MODE], [△] three times, [DEMUX F HEX V].

RECORD: Press [ARM].

REVIEW: Display Timing screen. Press [TIMING].

The display should look like Figure 10-54. The same information is sampled on inputs A7 through A0 and latched before sampling on AF through A8.

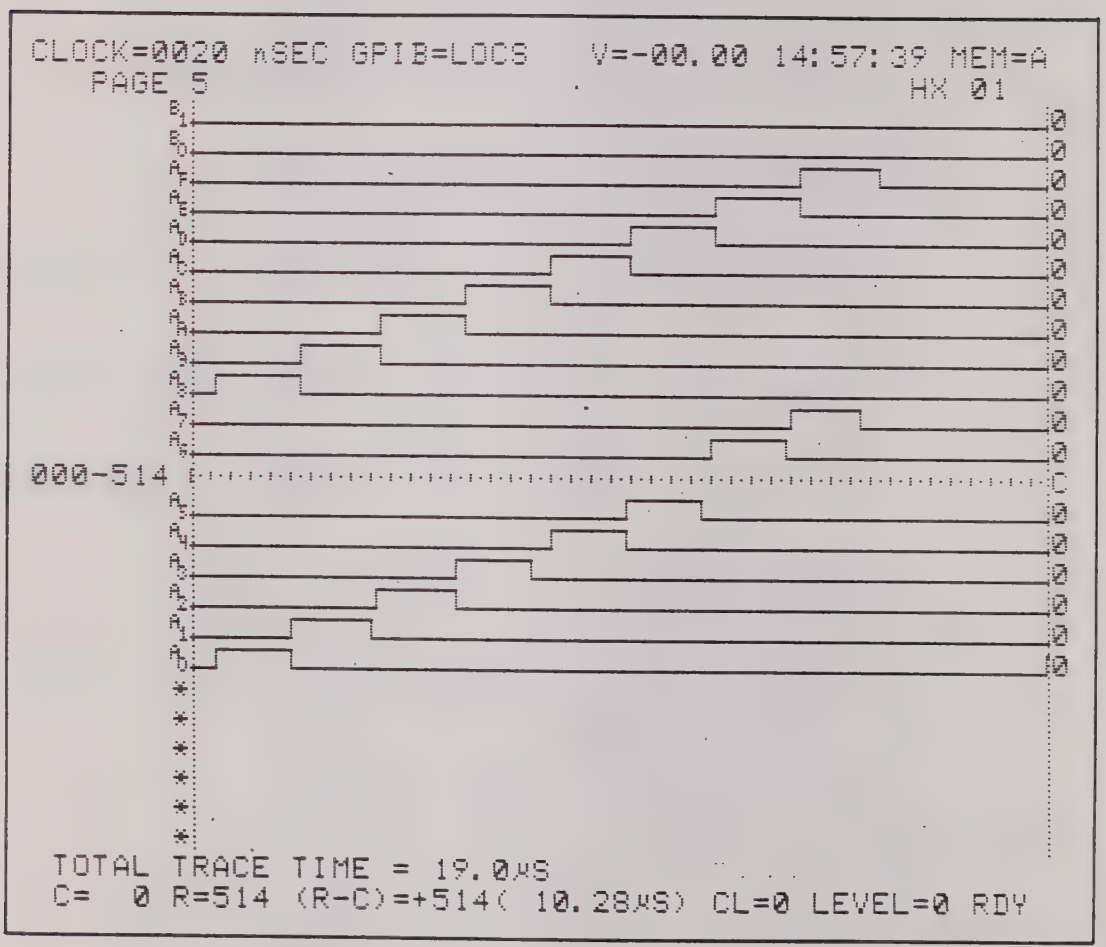


Figure 10-54. AF Through A8 Latched by AR↑.

SET UP: When AR↓ is used the A7 through A0 inputs also sent to AF through A8 are latched there by the enable signal AR↓.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+__)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↓ is used, the Timing display should look like Figure 10-55. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓.

SET UP: When AS↑ is used, the A7 through A0 inputs also sent to AF through A8 are latched there by the enable signal AS↑.

When AS↑ is used, the Timing display should look like Figure 10-56. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AS↑.

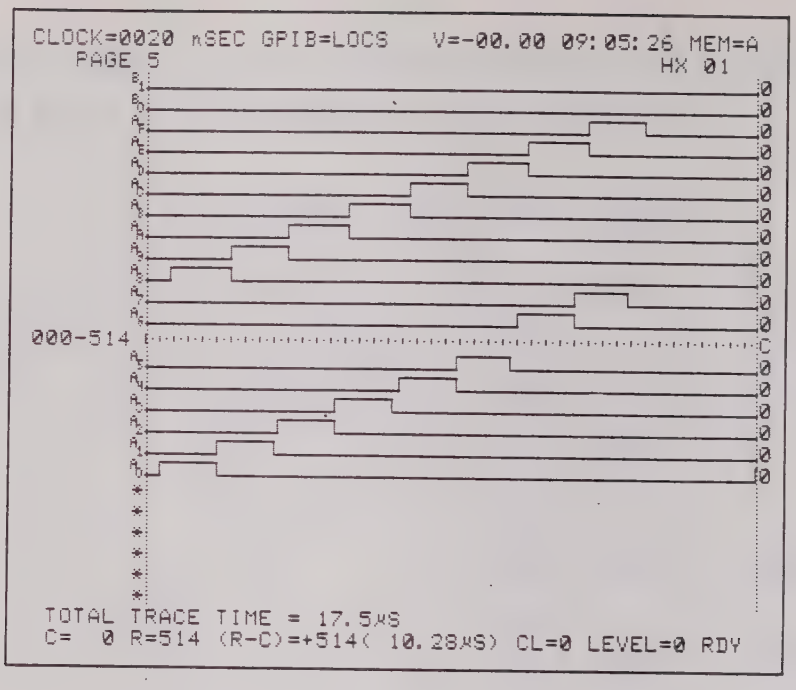


Figure 10-55. AF Through AS Latched by AR↓.

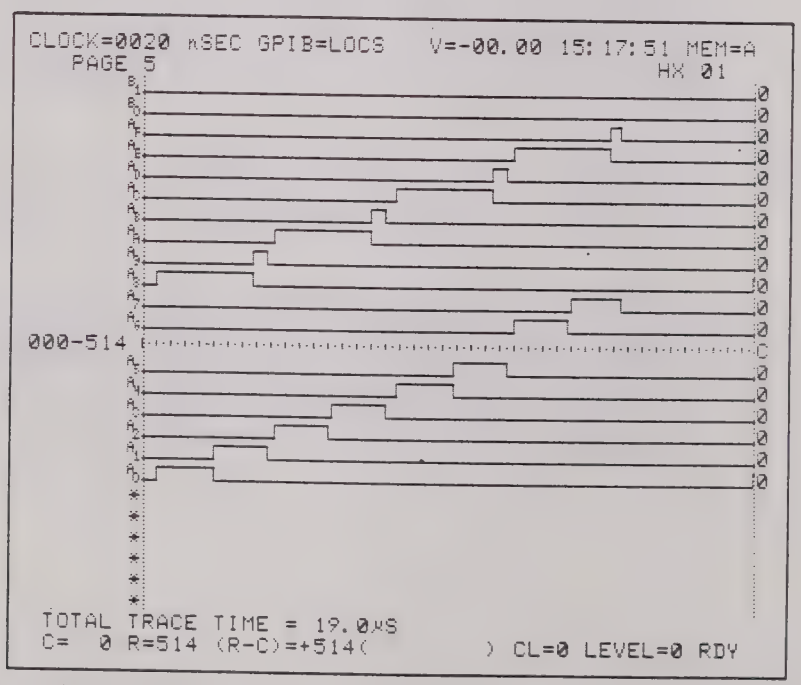


Figure 10-56. AF Through A8 Latched by AS↑.

SET UP: When AS↓ is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AS↓.

Change Clock Select display to the following:

ENABLE A = EXT (__·__·__) + (__+__+ AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] five times, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AS↓ is used, the Timing display should look like Figure 10-57. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AS↓.

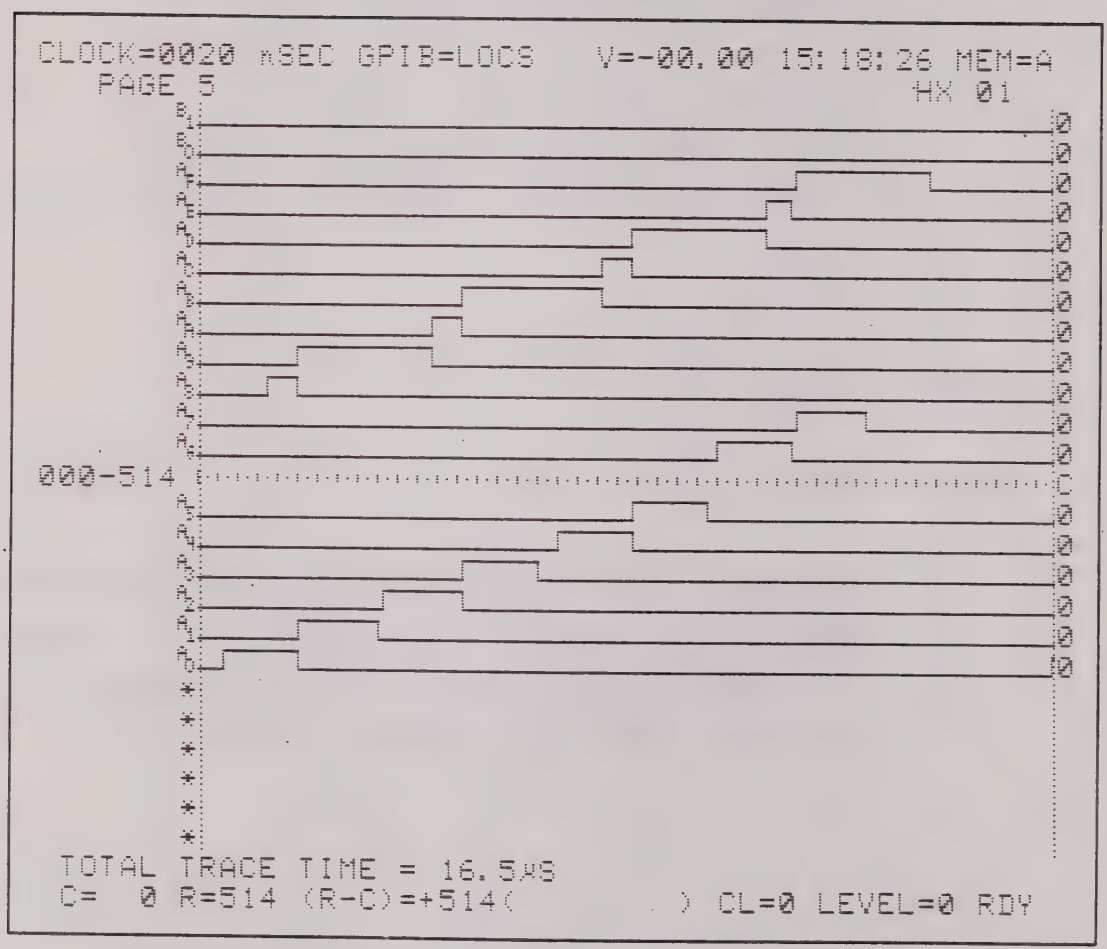


Figure 10-57. AF Through AS Latched by AS↓.

10.2.4.7 Demultiplex on a Combination of Enable Signals (AR↑ + AS↑, AR↓ + AS↑, AR↑ + AS↓, AR↓ + AS↓)

SET UP: The A7 through A0 inputs, also sent to AF through A8, are latched there by the enable signal AR↑, AS↑. Change Clock Select display to the following:

ENABLE A = EXT (__•__• AR↑) + (__+__+ AS↑)

Press [CLOCK SELECT], [+ ▽ SET] four times, [+ ▷] twice, [Hx1 0 G], [+ ▷] three times, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Display the Timing screen. Press [TIMING].

The display should look like Figure 10-58. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↑ + AS↑.

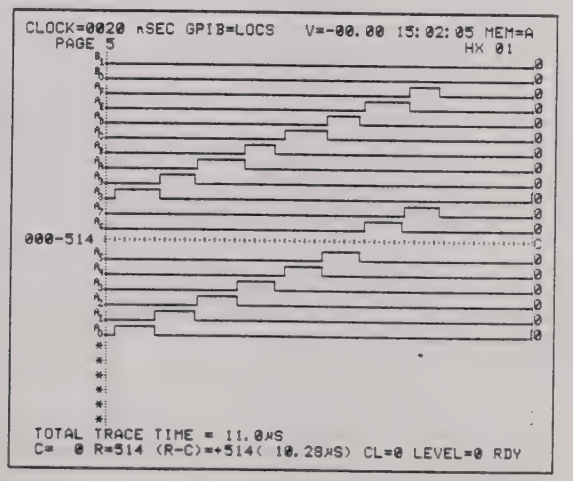


Figure 10-58. AF Through A8 Latched by AR↑ + AS↑.

SET UP: When AR↓ + AS↑ is used, the A7 through A0 inputs, also sent to AF through A8, are latched there by the enable signal AR↓ + AS↑.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+ AS↑)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↓ + AS↑ is used, the display should look like Figure 10-59. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓ + AS↑.

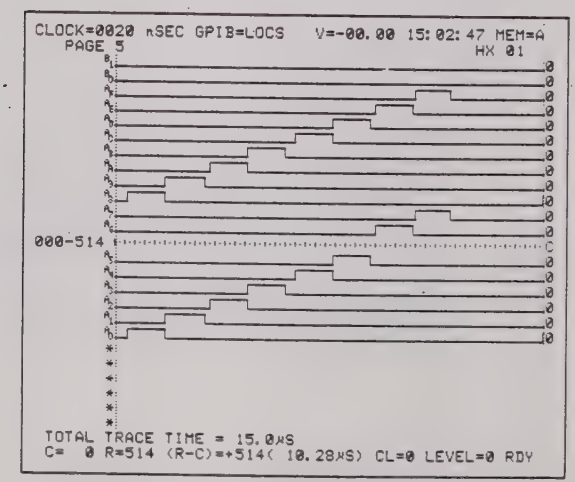


Figure 10-59. AF Through A8 Latched by AR↓ + AS↑.

SET UP: When AR↑ + AS↓ is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AR↑ + AS↓.

When AR↑ + AS↓ is used, the Timing display should look like Figure 10-60. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↑ + AS↓.

SET UP: When AR↓ + AS↓is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AR↓ + AS↓.

When AR↓ + AS↓ is used, the Timing display should look like Figure 10-61. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓ + AS↓.

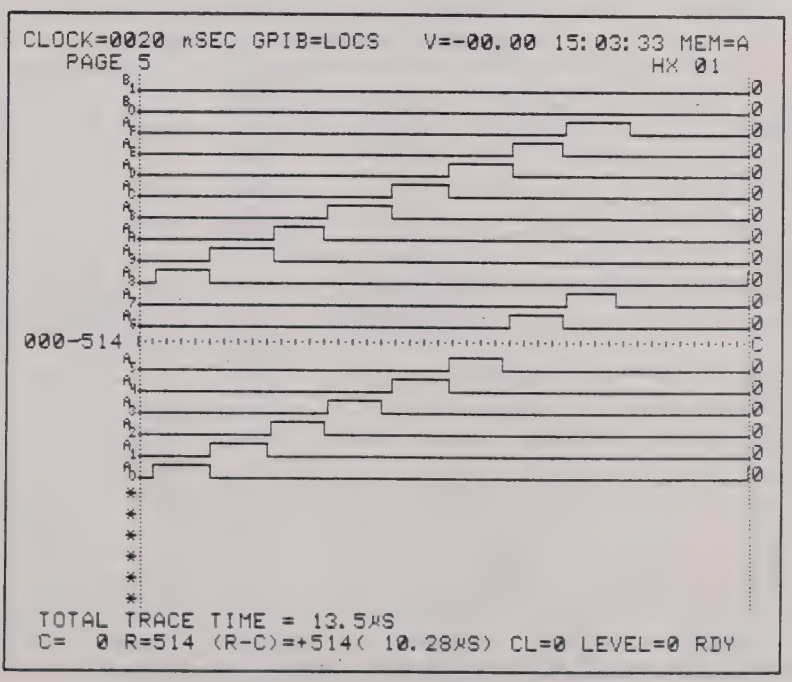


Figure 10-60. AF Through AS Latched by AR↑ + AS↓.

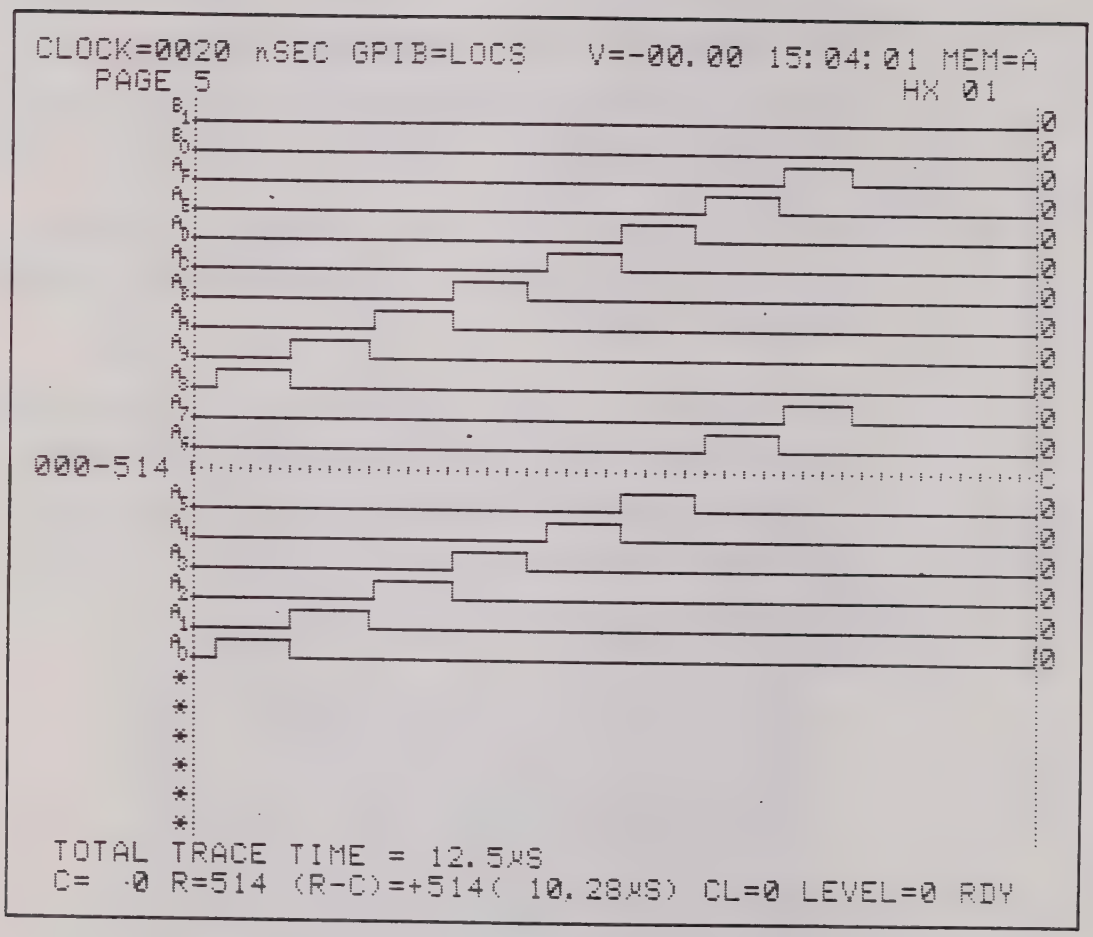


Figure 10-61. AF Through A8 Latched by AR↓ + AS↓.

10.2.5 TRACE CONTROL

The following are specific examples of the basic building blocks of trace control. There are some minor variations in some of the commands. (For example, TRACE IF DATA = T is often substituted for TRACE NEVER to better illustrate the recording process.) You may also notice some difference between a figure and what is displayed on your screen. This is due to remaining values from previous trace control routines. Specifically, if a command is NEVER or ALWAYS, then the value of its associated word recognizer is ignored, as if it were "don't care." Similarly, if DELAY is not used in any of a level's commands, then the specified delay value is ignored, as if it were "zero."

10.2.5.1 **Fill Memory with Samples from Anywhere in Data Stream**

SET UP: Unplug the A7 through A0 probe and connect the AF through A8 probe to PROBE TEST. See setup guide in Figure 10-62.

Display Clock Select screen.

Press [CLOCK SELECT] , [Hx3 1 H] , [▽ SET] twice, [▷] five times, [Hx6 2 I] .

Display Input Mode screen.

Press [INPUT MODE] , [△] , [Hx3 1 H] , [△] twice, [SAMPLE C S] .

Display Data Format screen.

Press [DATA FORMAT] , [Hx12 3 J] , [▽ SET] twice, [ASCII A Q] , [DEMUX F V HEX] ,

[ASCII A Q] , [LATCH E U OCTAL] , [ASCII A Q] , [GLITCH D T DECIMAL] , [ASCII A Q] , [SAMPLE C S] ,

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #51.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AzAa
A T 2	AzAA
S 1	AaA9
LSB	AcAa

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA = D and Sample Count ≤ Delay
8	If DATA = D and Sample Count < > Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

515 SEQUENTIAL SAMPLES WILL BE RECORDED BEGINNING AT A RANDOM LOCATION.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP _____
S = _____

(___) JUMP TO ___ (O-F) _____
J = _____

(___) ADVANCE _____
A = _____

(___) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP _____
S = _____

(___) JUMP TO ___ (O-F) _____
J = _____

(___) ADVANCE _____
A = _____

(___) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP _____
S = _____

(___) JUMP TO ___ (O-F) _____
J = _____

(___) ADVANCE _____
A = _____

(___) TRACE _____
T = _____

COMMENTS

Figure 10-62. Setup Guide: Fill Memory with Samples from Anywhere in Data Stream (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #S.1.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXT. SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence.
1	OCTAL — Fixed octal format & CF-A0 sequence.
2	BINARY — Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN — Any radix, any sequence.
4	MIXED CF-A0 SEQN — Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS — Fixed disassembled µP code format, one of RTE-816 emulator. OR
5	DEVICE NOT AVAILABLE — No RTE-816 emulator.

CLOCKING NOTES

SAMPLE CLOCK CHOICES	
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

ENABLE CLOCK CHOICES	
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

MODE & DESCRIPTIONS	
0	INTERNAL — All sections are sampled at the internal clock rate. Section A - Section B - Section C - Internal clock period.
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A - Section B - Section C - Master external.
2	EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C - Master external or internal clock period or 10ns.
4	MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C - Master external or internal or 10ns.
5	INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and/or Section C - Internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (1) ARM MODE: AUTO

LIMITS = _____ TO _____ (CURSORS C: 0-612 R: 0-612)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-62. Setup Guide: Fill Memory with Samples from Anywhere in Data Stream (Sheet 2 of 2).

[▽] SET, [A] Q (ASCII, A), [B] R (BINARY, B), [A] Q (ASCII, A), [A] Q (ASCII, A), [A] Q (ASCII, A),
[9] P (EBCDIC, ECL), [A] Q (ASCII, A), [8] O (PAGE↑, TTL).

Display Trace Control screen.

Press [ ] (TRACE CONTROL), [▽] SET, [3] J (Hx12), [▽] SET, [*] SPACE (DON'T CARE)
twice.

The Trace Control screen should look like Figure 10-63.

RECORD: Press [ ] (ARM).

REVIEW: Display Timing screen.

Press [ ] (TIMING), [3] J (Hx12). You should be on page 4.

Observe how the pattern starts in a different location for every recording. This is because no unique starting or stopping location is specified for capturing the information; it happens randomly.

Stop.

Press [ ] (STOP).

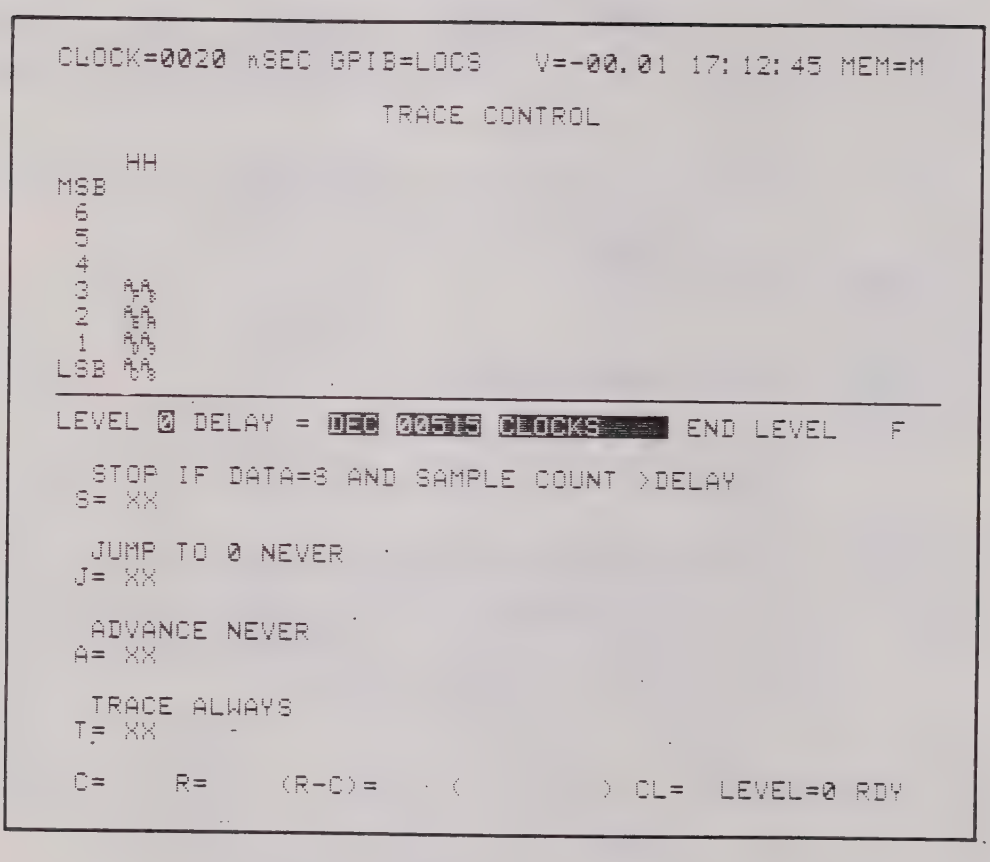


Figure 10-63. Fill Memory From Anywhere in the Data Stream.

10.2.5.2 Record What Happens Immediately After an Event

SET UP: Change the trace control program to be as in Figures 10-64 and 10-65.

Press [TRACE CONTROL], [▽ SET], [2 Hx6 I], [▽ SET] twice, [0 Hx1 G], [▽ SET], [0 Hx1 G], [1 Hx3 H], [▽ SET], [0 Hx1 G], [▽ SET], [0 Hx1 G], [1 Hx3 H], [▽ SET], [1 Hx3 H], [▷] twice, [5 V24 L], [1 Hx3 H], [1 Hx3 H], [▽ SET], [5 V24 L].

RECORD: Press [ARM].

REVIEW: Display Timing screen. Press [TIMING].

Notice that the pattern consistently starts in the same location.

Press [DATA] to see the same thing in the Data Domain display. Stop. Press [STOP].

This display should look like Figure 10-66. Note that the event of interest is the word 01 at location 000; it was captured by the trace control conditions on level 0, as indicated by CL = 0.

Press [▷] (see Figure 10-67).

Note that this and all subsequent words in memory were captured by trace control level 1.

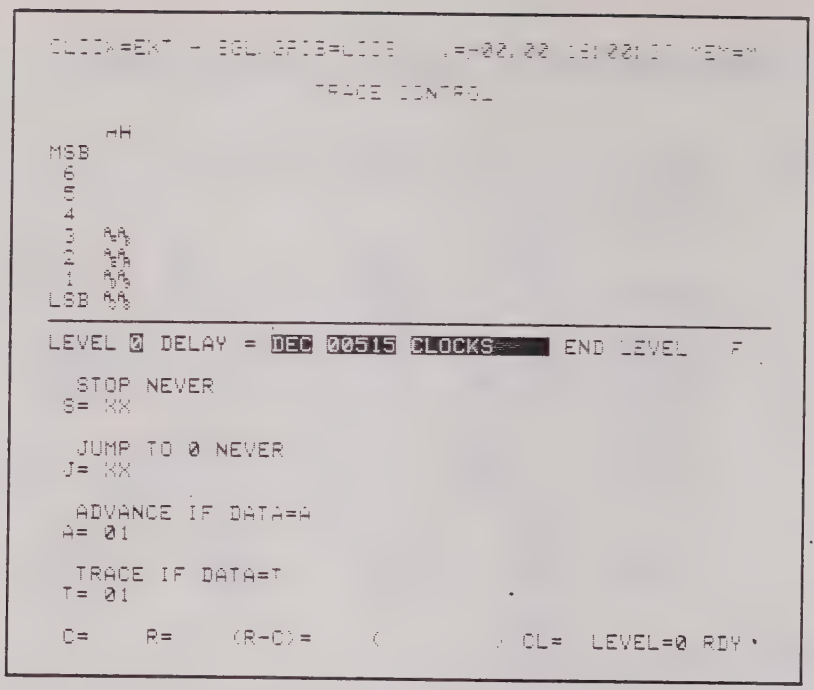


Figure 10-64. First Level, Record Immediately After Event 01.

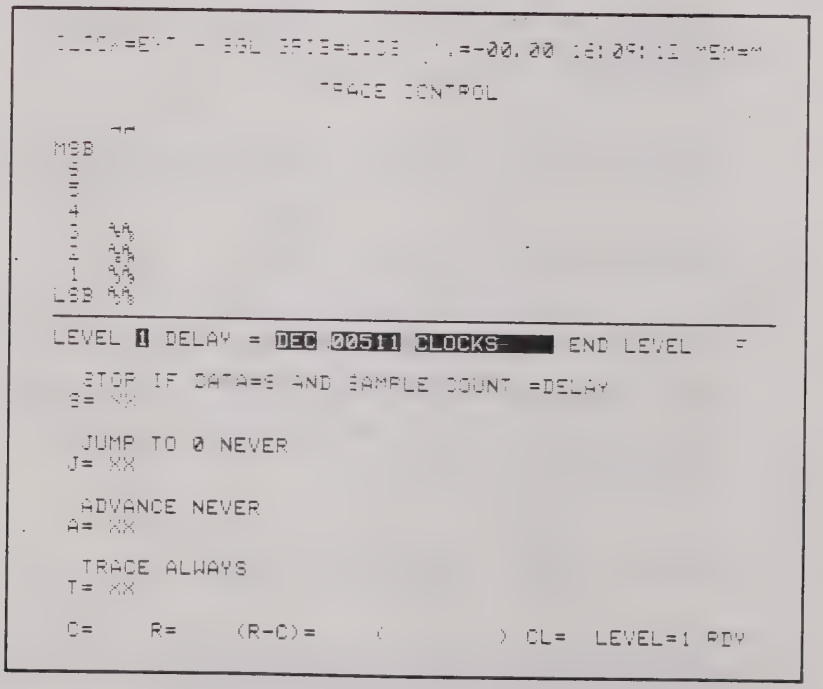
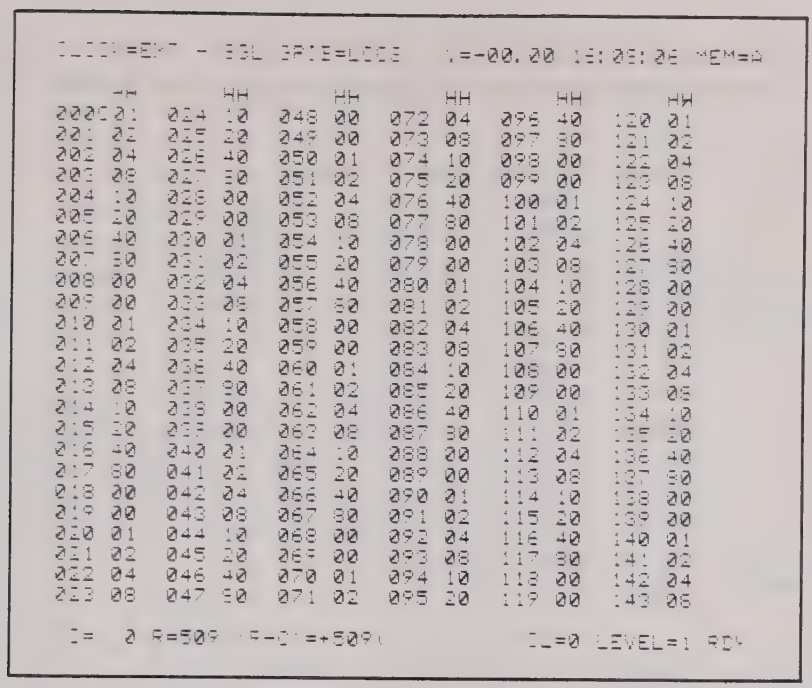


Figure 10-65. Second Level, Record Immediately After Event 01.

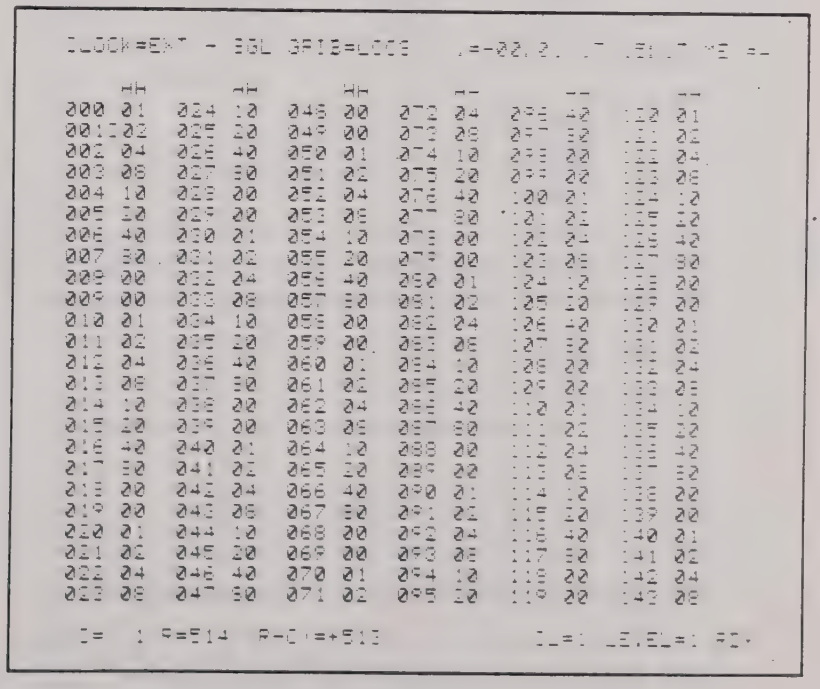


```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 16:08:06 MEM=A

     HH       HH       HH       HH       HH       HH
000C01   024 10   048 00   072 04   096 40   120 01
001 02   025 20   049 00   073 08   097 80   121 02
002 04   026 40   050 01   074 10   098 00   122 04
003 08   027 80   051 02   075 20   099 00   123 08
004 10   028 00   052 04   076 40   100 01   124 10
005 20   029 00   053 08   077 80   101 02   125 20
006 40   030 01   054 10   078 00   102 04   126 40
007 80   031 02   055 20   079 00   103 08   127 80
008 00   032 04   056 40   080 01   104 10   128 00
009 00   033 08   057 80   081 02   105 20   129 00
010 01   034 10   058 00   082 04   106 40   130 01
011 02   035 20   059 00   083 08   107 80   131 02
012 04   036 40   060 01   084 10   108 00   132 04
013 08   037 80   061 02   085 20   109 00   133 08
014 10   038 00   062 04   086 40   110 01   134 10
015 20   039 00   063 08   087 80   111 02   135 20
016 40   040 01   064 10   088 00   112 04   136 40
017 80   041 02   065 20   089 00   113 08   137 80
018 00   042 04   066 40   090 01   114 10   138 00
019 00   043 08   067 80   091 02   115 20   139 00
020 01   044 10   068 00   092 04   116 40   140 01
021 02   045 20   069 00   093 08   117 80   141 02
022 04   046 40   070 01   094 10   118 00   142 04
023 08   047 80   071 02   095 20   119 00   143 08

 C=  0 R=509 (R-C)=+509)          CL=0 LEVEL=1 RDY
```

Figure 10-66. Event 01 Recorded by Trace Level 0.



```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.0[illegible] [illegible] MEM=A

     HH       HH       HH       HH       HH       HH
000 01   024 10   048 00   072 04   096 40   120 01
001C02   025 20   049 00   073 08   097 80   121 02
002 04   026 40   050 01   074 10   098 00   122 04
003 08   027 80   051 02   075 20   099 00   123 08
004 10   028 00   052 04   076 40   100 01   124 10
005 20   029 00   053 08   077 80   101 02   125 20
006 40   030 01   054 10   078 00   102 04   126 40
007 80   031 02   055 20   079 00   103 08   127 80
008 00   032 04   056 40   080 01   104 10   128 00
009 00   033 08   057 80   081 02   105 20   129 00
010 01   034 10   058 00   082 04   106 40   130 01
011 02   035 20   059 00   083 08   107 80   131 02
012 04   036 40   060 01   084 10   108 00   132 04
013 08   037 80   061 02   085 20   109 00   133 08
014 10   038 00   062 04   086 40   110 01   134 10
015 20   039 00   063 08   087 80   111 02   135 20
016 40   040 01   064 10   088 00   112 04   136 40
017 80   041 02   065 20   089 00   113 08   137 80
018 00   042 04   066 40   090 01   114 10   138 00
019 00   043 08   067 80   091 02   115 20   139 00
020 01   044 10   068 00   092 04   116 40   140 01
021 02   045 20   069 00   093 08   117 80   141 02
022 04   046 40   070 01   094 10   118 00   142 04
023 08   047 80   071 02   095 20   119 00   143 08

 C=  1 R=514 (R-C)=+513)          CL=1 LEVEL=1 RDY
```

Figure 10-67. Words Recorded by Trace Level 1.

10.2.5.3 Record What Happens Immediately Before an Event

SET UP: Change the arm mode to manual.

Press [INPUT MODE] , [△] , [Hx1 0 G] .

Change trace control.

Press [TRACE CONTROL] , [▽ SET] , [Hx1 0 G] , [▽ SET] , [Hx1 0 G] , [Hx3 1 M] , [▽ SET] twice, [Hx6 2 I] , [▽ SET] twice, [Hx3 1 M] .

RECORD: Press [ARM] .

REVIEW: Show the Data display. Press [DATA] .

Note that CL = F and that the data are all zeros.

Press [SHIFT] , [◁ SET] , [V24 5 L] , [Hx1 0 G] , [Hx1 0 G] , [DATA] .

Press [▷] until CL = 0 (see Figure 10-68).

This is the first traced sample. Tracing continued until 01 occurred and then stopped. Since the Probe Test pattern generator output is continuous and your press of [ARM] is asynchronous with it, tracing can start at any point in the cycle. However, since the pattern repeats every ten sample clocks, a maximum of nine words can occur before the S = 01 condition is met. To see how the first word sampled can vary, press [ARM] again and then [◁ SET] , or [▷] .

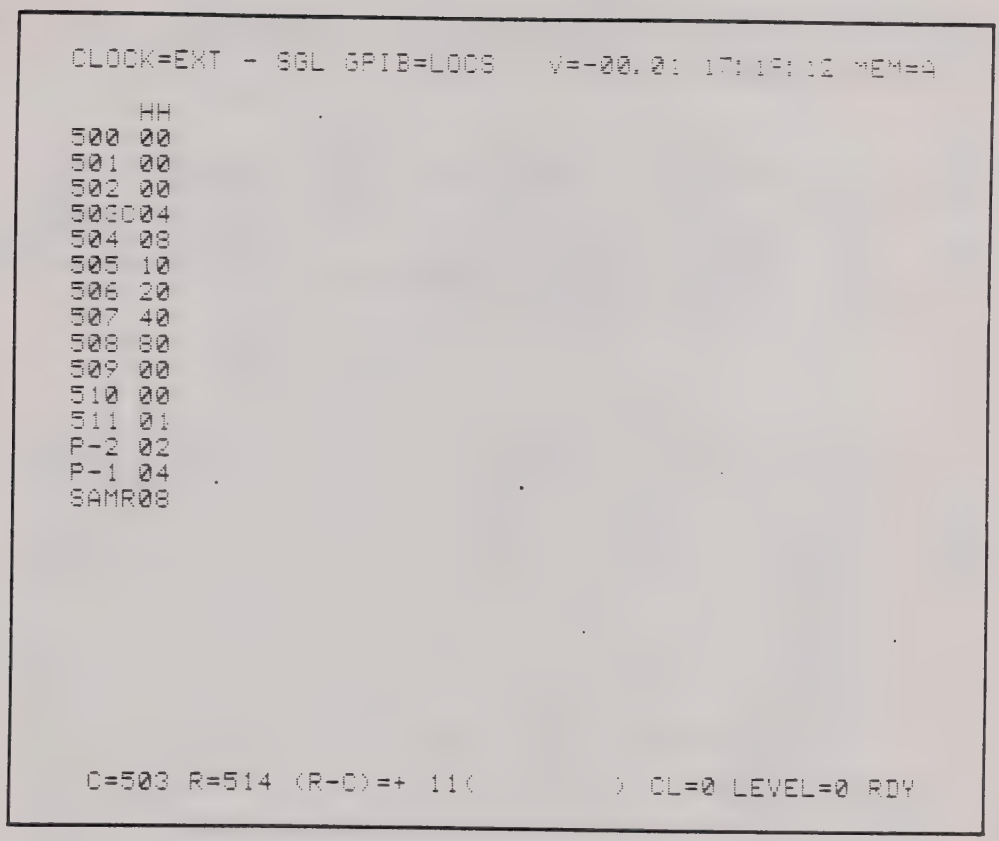


Figure 10-68. First Traced Sample.

This finds the first word captured on level 0 (indicated by CL = 0). Note that location 511 always holds the word 01. Repeat this process several times.

Press until C is at location P-2 (see Figure 10-69).

Note that CL = ?. These last three locations (also referred to as 512, 513, and 514) are the pipeline and sample register contents -- words not yet evaluated by the trace control circuitry.

```
CLOCK=EXT - SGL GPIB=LOCS   V=-00.01 17:19:12 MEM=A

     HH
500 00
501 00
502 00
503 04
504 08
505 10
506 20
507 40
508 80
509 00
510 00
511 01
P-2 02
P-1 04
SAMP 08

C=512 R=514 (R-C)=+  2(          CL=? LEVEL=0 PI:
```

Figure 10-69. Last Three Displayed Words Sampled.

10.2.5.4 **Record What Happens Around an Event**

SET UP: The following will put an event of interest in the middle of memory. Specifically, to put word 01 in sample location 246, the stop of tracing must be delayed by 265(511 - 246) sample clocks. Change the trace control program.

Press [TRACE CONTROL], [▽ SET], [▽ SET] twice, [Hx1 0 G], [▽ SET] three times, [Hx3 1 M], [▷] twice, [Hx6 2 I], [V12 6 M], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx6 2 I], [Hx12 3 J], [V12 6 M], [DATA].

Press [▷] until C is at location 246.

The display will look similar to Figure 10-70. The event of interest, 01, has been placed at the specified mid-memory location 246. Note that 01 was recorded there by trace level 0. The following 265 words were recorded by trace level 1. (Again, because of Probe Test's repetitive pattern, only up to nine words could have been recorded on level 0 before 01 occurred.)

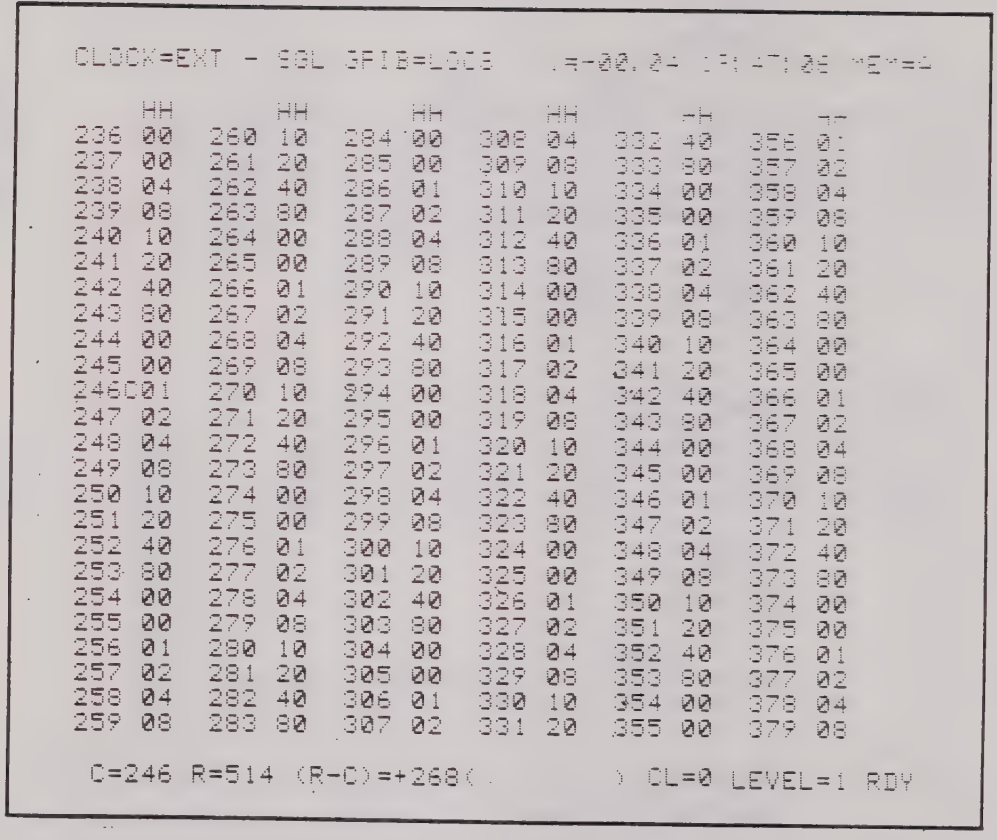


Figure 10-70. Event Placed at Location 246.

10.2.5.5 **Record What Happens Long After an Event**

SET UP: Use the setup guide of Figure 10-71. This will capture a memory full of information long after an event, as well as the event itself, yet without the intervening information.

Press [TRACE CONTROL], [▽ SET] five times, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▷] twice, [V24 5 L], [Hx3 1 H], [V24 5 L], [▽ SET], [▽ SET] twice, [V24 5 L], [▽ SET] twice [Hx6 2 I], [▽ SET], [Hx6 2 I], [▷] twice, [V24 5 L], [Hx3 1 H], [Hx1 0 G], [▽ SET], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [DATA].

The display should look like Figure 10-72. Recording the words in locations 002 to 511 was delayed from recording the word at location 001 by 515 sample clocks. The intervening words were not recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5120 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AFAB
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level ...
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions:

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count < > Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = A
T = 0 1

COMMENTS

ONLY 01 IS TRACED INTO MEMORY. AT ITS OCCURANCE, TRACE CONTROL ADVANCES TO LEVEL 1.

LEVEL 1 (0-F) DELAY = DEC 515 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = X X

(2) TRACE NEVER
T = X X

COMMENTS

NOTHING IS TRACED IN THIS LEVEL IT MERELY WAITS FOR 515 CLOCKS TO OCCUR BEFORE ADVANCING.

LEVEL 2 (0-F) DELAY = DEC 510 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(5) STOP IF DATA = S AND SAMPLE COUNT = DELAY
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

THE REST OF MEMORY IS FILLED WITH THE NEXT 510 SEQUENTIAL SAMPLES.

LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(___) STOP
S =

(___) JUMP TO ___ (0-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

COMMENTS

Figure 10-71. Setup Guide: Record What Happens Around an Event (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.2 D

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____ ● _____ ● AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = (_____ ● _____ ● _____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Preset hex format & CF-A0 sequence.
1	OCTAL Preset octal format & CF-A0 sequence.
2	BINARY Preset binary format & CF-A0 sequence.
3	MIXED USER BSON Any mode, any sequence.
4	MIXED CF-A0 BSON Any mode, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Preset decimal/octal/hex mode format, uses # RTE-S10 mnemonics. OR
6	DEVICE NOT AVAILABLE No RTE-S10 assigned.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate Section A + Section B + Section C + Internal clock period.

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate Section A + Section B + Section C + Master (simultaneous)

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C = Master external or internal clock period or 10ns

4 MIXED MULTI PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B, and or Section C = Master external or internal or 10ns

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns Section A, Section B, and or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ___ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↑	↑	↑	↑	↑	↑	↑	↑	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-71. Setup Guide: Record What Happens Around an Event (Sheet 2 of 2).

```
CLOCK=EXT - SGL GPIB=LOC8    V=-00.04 19:54:07 MEM=A

     HH        HH        HH        HH        HH        HH
000C00   024 00   048 04   072 40   096 01   120 10
001 01   025 00   049 08   073 80   097 02   121 20
002 40   026 01   050 10   074 00   098 04   122 40
003 80   027 02   051 20   075 00   099 08   123 80
004 00   028 04   052 40   076 01   100 10   124 00
005 00   029 08   053 80   077 02   101 20   125 00
006 01   030 10   054 00   078 04   102 40   126 01
007 02   031 20   055 00   079 08   103 80   127 02
008 04   032 40   056 01   080 10   104 00   128 04
009 08   033 80   057 02   081 20   105 00   129 08
010 10   034 00   058 04   082 40   106 01   130 10
011 20   035 00   059 08   083 80   107 02   131 20
012 40   036 01   060 10   084 00   108 04   132 40
013 80   037 02   061 20   085 00   109 08   133 80
014 00   038 04   062 40   086 01   110 10   134 00
015 00   039 08   063 80   087 02   111 20   135 00
016 01   040 10   064 00   088 04   112 40   136 01
017 02   041 20   065 00   089 08   113 80   137 02
018 04   042 40   066 01   090 10   114 00   138 04
019 08   043 80   067 02   091 20   115 00   139 08
020 10   044 00   068 04   092 40   116 01   140 10
021 20   045 00   069 08   093 80   117 02   141 20
022 40   046 01   070 10   094 00   118 04   142 40
023 80   047 02   071 20   095 00   119 08   143 80

 C=  0 R=514 (R-C)=+514(          ) CL=F LEVEL=2 RD+
```

Figure 10-72. Recording of Selected Words.

Press [▷] . Note that CL = F changes to CL = 0; 01 was recorded by trace level 0. Press [▷] again.

Note that CL = 2; the next recorded sample was traced by level 2. Nothing was recorded during level 1. Although 515 samples (1 memoryful) flowed through the analyzer between trace control levels 0 and 2, none of them were stored in memory.

10.2.5.6 Capture a Segment of Samples: Record from Here to There

SET UP: Only a part of one cycle of the Probe Test pattern (the word sequence 01, 02, 04, 08, 10, 20, 40, 80) will be captured. See setup guide in Figure 10-73. Change the trace control program.

Press [TRACE CONTROL] , [▽ SET] four times, [Hx1 0 G] , [Hx3 1 H] , [▽ SET] twice, [Hx1 0 G] , [Hx3 1 H] , [▽ SET] , [Hx3 1 H] , [▽ SET] three times, [Hx1 0 G] , [▽ SET] , [PAGE 8 O TTL] , [Hx1 0 G] , [▽ SET] , [Hx3 1 H] , [▽ SET] , [Hx6 2 I] , [▽ SET] , [Hx3 1 H] , [▽ SET] four times, [Hx6 2 I] .

RECORD: Press [ARM] .

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 51.3 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3
A T 2
S 1
LSB

3 AF AB
2 AE A1
1 AD A9
0 AC A8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level: —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count Delay
4	If DATA = D and Sample Count Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count = Delay
7	If DATA = D and Sample Count = Delay
8	If DATA = D and Sample Count Delay

ID = S, J, A, or T, which are assigned by command type I

TRACE CONTROL

LEVEL 0 (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS

TRACE CONTROL WAITS FOR 01 TO OCCUR, THEN TRACES IT AND ADVANCES.

LEVEL 1 (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 8 0

(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED UP UNTIL 80 OCCURS, THEN TRACE CONTROL ADVANCES.

LEVEL 2 (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(2) TRACE NEVER
T = X X

COMMENTS

NO MORE SAMPLES ARE TRACED AND THE RECORDING PROCESS STOPS, SINCE THE DESIRED SEGMENT HAS BEEN RECORDED.

LEVEL ___ (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(___) STOP
S =

(___) JUMP TO ___ (0-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

COMMENTS

Figure 10-73. Setup Guide: Capture a Segment of Samples: Record from Here to There (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.3

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE - PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____ ● _____ ● AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = (_____ ● _____ ● _____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Read hex format & CF-A0 sequence.
1	OCTAL Read octal format & CF-A0 sequence.
2	BINARY Read binary format & CF-A0 sequence.
3	MIXED USER SIGN Any radix, any sequence.
4	MIXED CF-A0 SIGN Any radix, Read CF-A0 sequence.
5	DEVICE MNEMONICS Read decommented .df data format, only if RTE-816 attached. OR
6	DEVICE NOT AVAILABLE No RTE-816 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate Section A - Section B - Section C - Internal clock period.

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate Section A - Section B - Section C - Master (strobe).

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master/incremental or internal clock period or 10ns.

4 MIXED MULTI PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (strobe) or internal or 10ns.

5 INTERNAL EXTENDED
Each section can be sampled at the Internal clock rate or 10ns Section A, Section B, and or Section C - Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = CURSORS _____ TO _____ C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	+	+	+	+	+	+	+	+	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

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Figure 10-73. Setup Guide: Capture a Segment of Samples: Record from Here to There (Sheet 2 of 2).

REVIEW: Press [SHIFT], [◁ SET], [5 L], [0 G], [3 J], [DATA], [▷].

The display should look like Figure 10-74. The first word of the pattern segment was captured by level 0 and the following nine by level 1.

Press [▷] to location 511 (see Figure 10-75).

The segment was captured on levels 0 and 1; recording stopped on level 2 (as indicated by LEVEL = 2 RDY).

Press [TIMING] and move the Control Cursor [◁ SET] to verify that only one pattern was recorded.

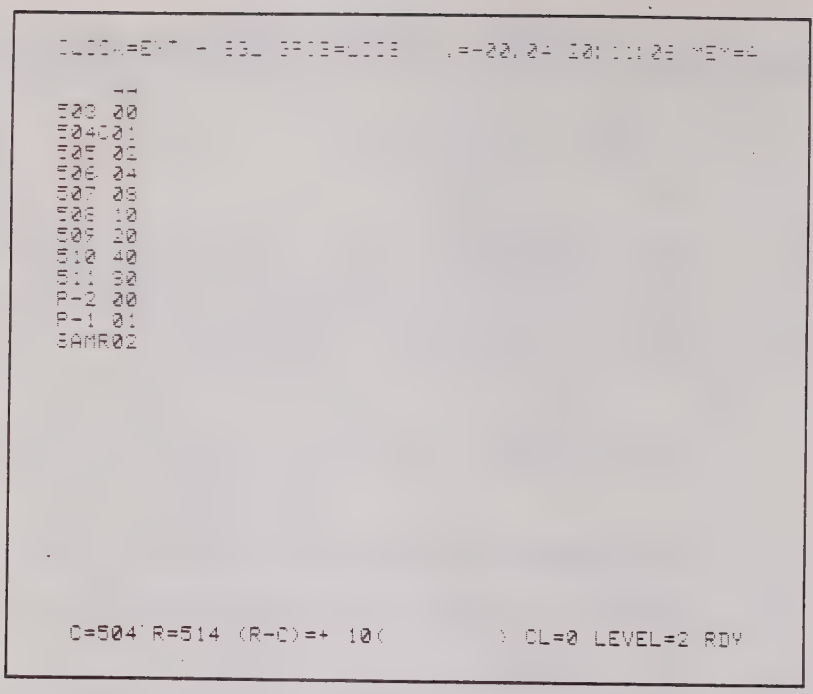


Figure 10-74. First Word (01) Recorded by Level 0.

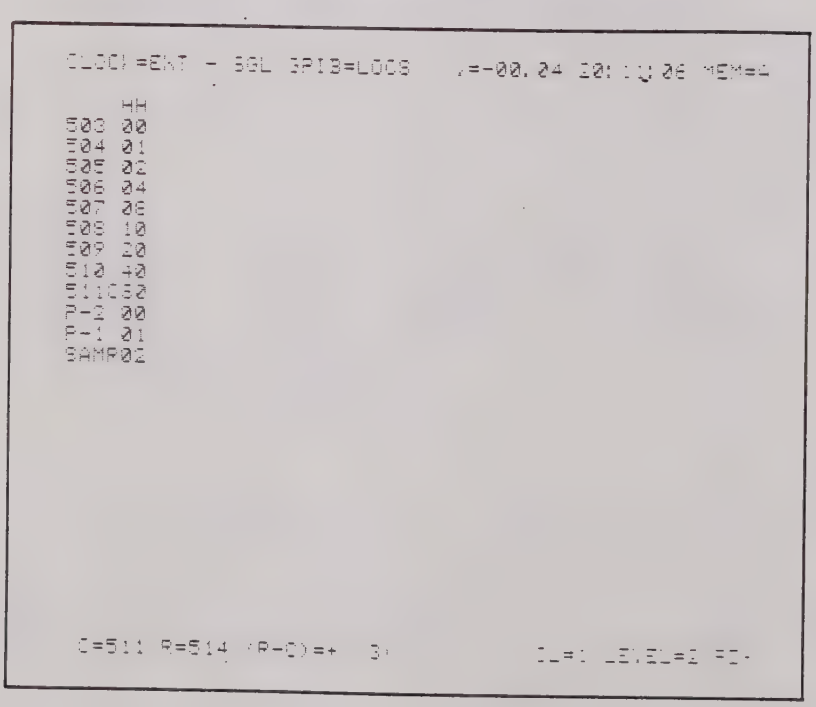


Figure 10-75. Words of Segment Recorded by Level 1.

10.2.5.7 Exclude Recording a Segment of Samples: Don't Record from Here to There

SET UP: To exclude capturing all the words between the first (01) and last (80) words of one cycle of the pattern, see setup guide in Figure 10-76.

Press [TRACE CONTROL] , [▽ SET] five times, [Hx3 1 M] , [▽ SET], [Hx3 1 M] , [▽ SET] five times, [Hx1 0 G] , [▽ SET], [PAGE 8 O TTL], [Hx1 0 G] , [▽ SET], [Hx6 2 I] , [▷] twice, [V24 5 L] , [Hx1 0 G] , [Hx1 0 G] , [▽ SET], [Hx12 3 J] , [▽ SET] five times, [Hx3 1 M] .

RECORD: Press [ARM] .

REVIEW: Press [SHIFT] , [◁ SET] , [Hx1 0 G] , [TIMING] .

This display should look like Figure 10-77. The six pulses between the first and last pulse of the pattern were not recorded in memory, although they were sampled into the analyzer. Notice the six missing pulses in the first cycle. They correspond to the excluded data words 02, 04, 08, 10, 20, and 40. Move the Control Cursor to verify the trace level on which each word was recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.4 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 8	
D N 5	
A P 4	
T U 3	AF A3
A T 2	AE A2
S 1	AD A1
LSB	AC A0

RADIX CHOICES: (B) BINARY (O) OCTAL (H) HEX. (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count - Delay
4	If DATA = D and Sample Count - Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count ≠ = Delay
7	If DATA = D and Sample Count - = Delay
8	If DATA = D and Sample Count - Delay

(D = S, J, A or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED UNTIL 01 OCCURS WHEN TRACE CONTROL THEN ADVANCES

LEVEL 1 (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 8 0

(0) TRACE IF DATA = T
T = 8 0

COMMENTS

THIS LEVEL WAITS FOR 80 TO OCCUR, TRACING NOTHING UNTIL IT DOES AND THEN ADVANCING.

LEVEL 2 (QUICK KEY, 0-F) DELAY = DEC (DEC/HEX) 500 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

FULL TRACING OF ALL SAMPLES RESUMES FOR 500 MORE CLOCKS.

LEVEL ___ (QUICK KEY, 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(___) STOP
S =

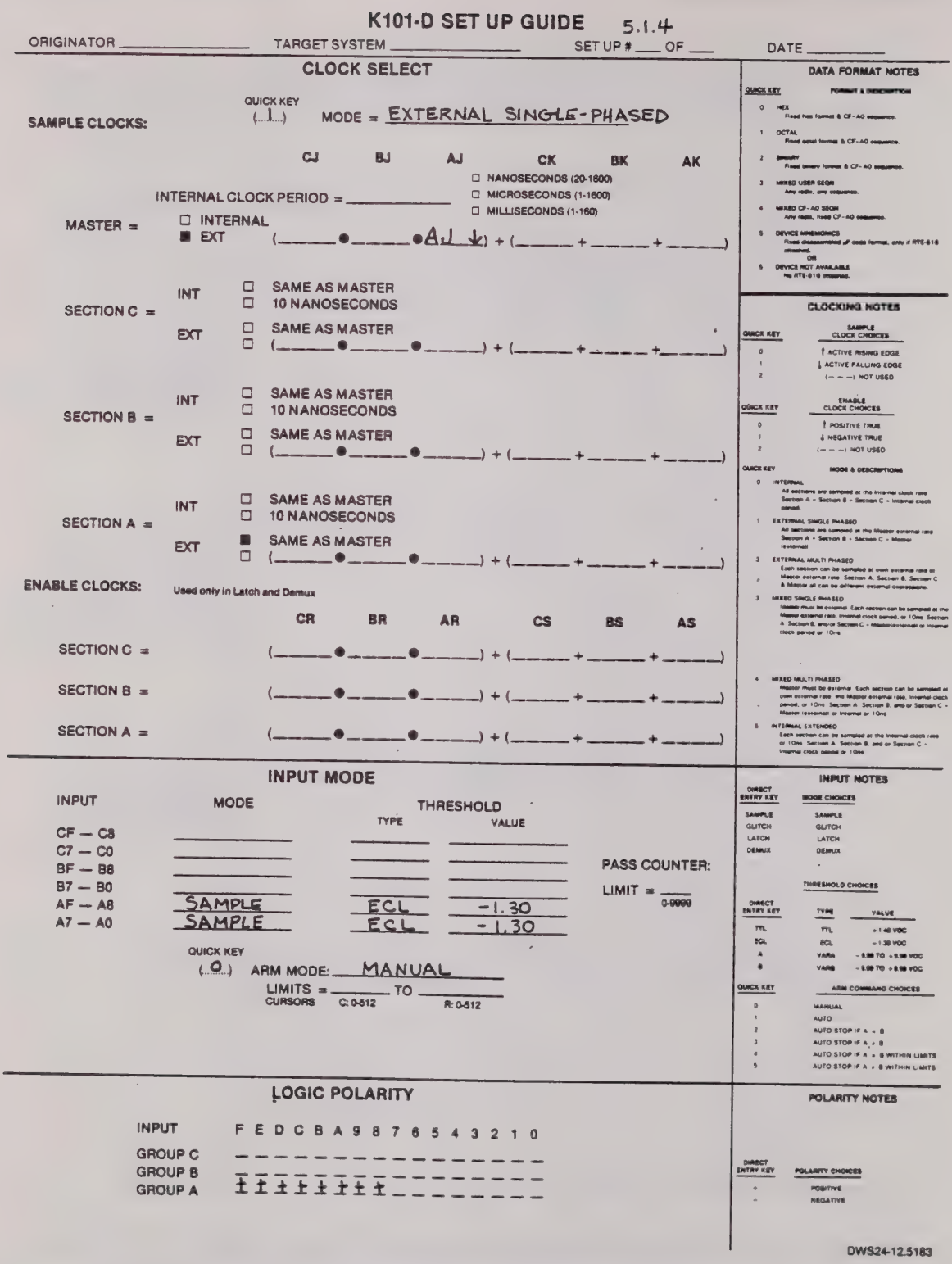
(___) JUMP TO ___ (0-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

COMMENTS

Figure 10-76. Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There (Sheet 1 of 2).



K101-D SET UP GUIDE 5.1.4

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____ • _____ • AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____ • _____ • _____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____ • _____ • _____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____ • _____ • _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ • _____ • _____) + (_____ + _____ + _____)

SECTION B = (_____ • _____ • _____) + (_____ + _____ + _____)

SECTION A = (_____ • _____ • _____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY — FORMAT & DESCRIPTION

0 HEX — Fixed hex format & CF-A0 sequence.

1 OCTAL — Fixed octal format & CF-A0 sequence.

2 BINARY — Fixed binary format & CF-A0 sequence.

3 MIXED USER SEQN — Any radix, any sequence.

4 MIXED CF-A0 SEQN — Any radix, fixed CF-A0 sequence.

5 DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 attached. OR

6 DEVICE NOT AVAILABLE — No RTE-816 attached.

CLOCKING NOTES

QUICK KEY — SAMPLE CLOCK CHOICES

0 ↑ ACTIVE RISING EDGE

1 ↓ ACTIVE FALLING EDGE

2 (— — —) NOT USED

QUICK KEY — ENABLE CLOCK CHOICES

0 ↑ POSITIVE TRUE

1 ↓ NEGATIVE TRUE

2 (— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL — All sections are sampled at the internal clock rate. Section A = Section B = Section C = Internal clock period.

1 EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master (external).

2 EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external clock rates.

3 MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C = Master(external) or internal clock period or 10ns.

4 MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or internal or 10ns.

5 INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and or Section C = Internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	_____	_____	_____
C7 — C0	_____	_____	_____
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ___ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY — MODE CHOICES

SAMPLE — SAMPLE

GLITCH — GLITCH

LATCH — LATCH

DEMUX — DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY — ARM COMMAND CHOICES

0 MANUAL

1 AUTO

2 AUTO STOP IF A = B

3 AUTO STOP IF A ≠ B

4 AUTO STOP IF A = B WITHIN LIMITS

5 AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY — POLARITY CHOICES

+ POSITIVE

– NEGATIVE

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Figure 10-76. Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There (Sheet 2 of 2).

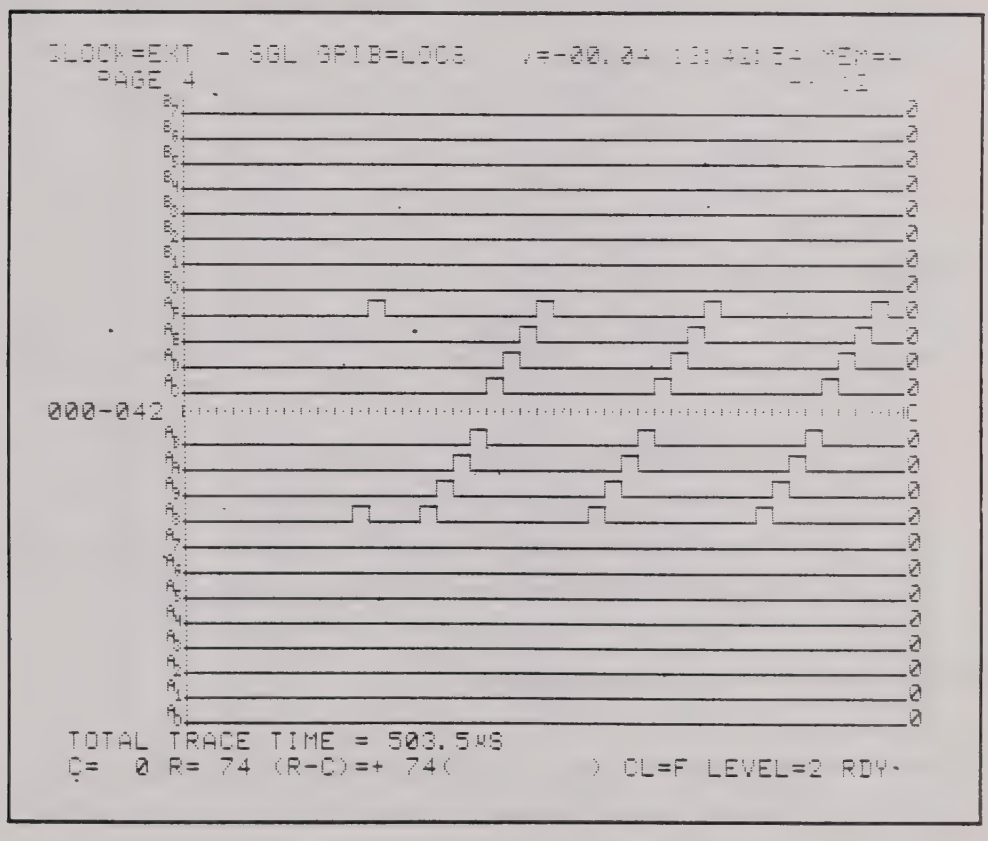

Figure 10-77. Six Pulses Sampled and Not Recorded.

10.2.5.8 Selectively Record Only One Kind of Sample for a Certain Number of Times

SET UP: To record only one memoryful of the word 01, change trace control.

Press [TRACE CONTROL], [▷], three times, [Hx3 1 H], [▽ SET], [V24 5 L], [▽ SET] three times, [Hx6 2 I], [▽ SET] twice, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx12 3 J], [V12 6 M], [DATA].

The display should look like Figure 10-78. Only 01s were recorded. P-2, P-1, and SAM show some of the other sampled words that flowed through the analyzer but did not meet the trace control TRACE conditions.

10.2.5.8 Follow a Path, Then Record

SET UP: Fill memory only after confirming that four words of the pattern occur in their proper sequence: 02, 08, 20, then 80. See setup guide in Figure 10-79.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [Hx6 2 I], [▽ SET], [Hx3 1 H], [▽ SET] four times, [Hx1 0 G], [PAGE 8 TTL], [▽ SET] twice, [Hx1 0 G], [PAGE 8 TTL],

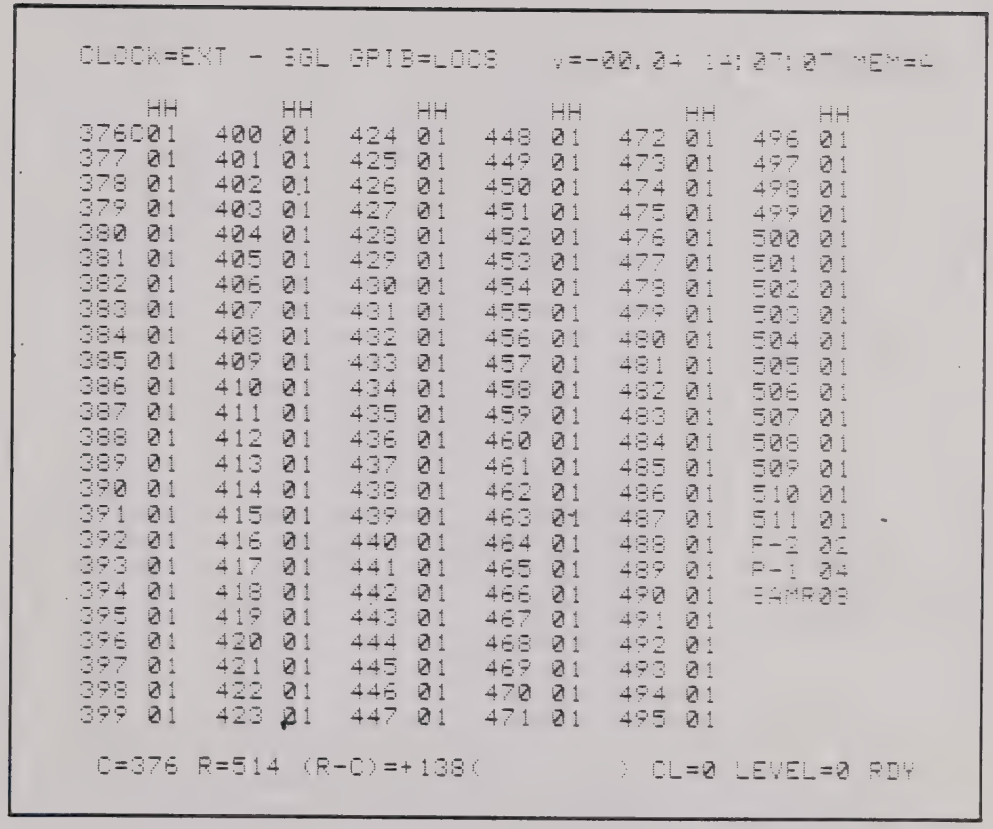

Figure 10-78. Word 01 Selected to be Recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.6 OF ___ DATE _____

QUICK KEY (See back for notes) (.3.) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AEAA
A T 2 AEAA
S 1 ADA1
LSB ACA0

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions.

Quick Key	Command Condition
0	If DATA = 0
1	Always
2	Never
3	If DATA = 0 and Sample Count - Delay
4	If DATA = 0 and Sample Count - Delay
5	If DATA = 0 and Sample Count = Delay
6	If DATA = 0 and Sample Count - = Delay
7	If DATA = 0 and Sample Count - = Delay
8	If DATA = 0 and Sample Count - Delay

(10 = S J A or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(.2.) STOP NEVER
S = X X

(.2.) JUMP TO 0 (O-F) NEVER
J = X X

(.0.) ADVANCE IF DATA = A
A = 0 2

(.0.) TRACE IF DATA = T
T = 0 2

COMMENTS
WAIT FOR 02, TRACE IT AND ADVANCE.

LEVEL 1 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(.2.) STOP NEVER
S = X X

(.2.) JUMP TO 0 (O-F) NEVER
J = X X

(.0.) ADVANCE IF DATA = A
A = 0 8

(.0.) TRACE IF DATA = T
T = 0 8

COMMENTS
WAIT FOR 08, TRACE IT AND ADVANCE.

LEVEL 2 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(.2.) STOP NEVER
S = X X

(.2.) JUMP TO 0 (O-F) NEVER
J = X X

(.0.) ADVANCE IF DATA = A
A = 2 0

(.0.) TRACE IF DATA = T
T = 2 0

COMMENTS
WAIT FOR 20, TRACE IT AND ADVANCE.

LEVEL 3 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(.2.) STOP NEVER
S = X X

(.2.) JUMP TO 0 (O-F) NEVER
J = X X

(.0.) ADVANCE IF DATA = A
A = 8 0

(.0.) TRACE IF DATA = T
T = 8 0

COMMENTS
WAIT FOR 80, TRACE IT AND ADVANCE.

Figure 10-79. Setup Guide: Follow a Path, Then Record (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.6 (cont.) ___ OF ___ DATE _____

QUICK KEY (see back for notes) (..3..) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AEAB
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count ≠ Delay
5	If DATA = D and Sample Count > Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA = D and Sample Count < Delay
8	If DATA = D and Sample Count ≤ Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

QUICK KEY LEVEL 4 (O-F) DELAY = DEC (DEC/HEX) 500 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(..3..) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(..2..) JUMP TO 0 (O-F) NEVER
J = X X

(..2..) ADVANCE NEVER
A = X X

(..1..) TRACE ALWAYS
T = X X

COMMENTS

TRACE ALL THE FOLLOWING 500 SAMPLES AND STOP.

QUICK KEY LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-79. Setup Guide: Follow a Path, Then Record (Sheet 2 of 2).

[▽ SET], [Hx6 2 I], [▽ SET], [Hx6 2 I], [▽ SET] twice,
[Hx1 0 G], [▽ SET], [Hx6 2 I], [Hx1 0 G], [▽ SET], [Hx1 0 G],
[▽ SET], [Hx6 2 I], [Hx1 0 G], [▽ SET], [Hx12 3 J],
[▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET],
[PAGE↑ 8 O TTL], [Hx1 0 G], [▽ SET], [PAGE↓ 4 K], [▷] twice,
[V24 5 L], [Hx1 0 G], [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [TIMING].

The display should look like Figure 10-80. The first four pulses had to occur in their proper sequence before the following pulses could be recorded.

Press [DATA], then press [▷] slowly ten times,

noting the cursor level of each word (see Figure 10-81). The words 02, 08, 20, and 80 were traced on levels 0, 1, 2, and 3, respectively, before the following data could be recorded by level 4.

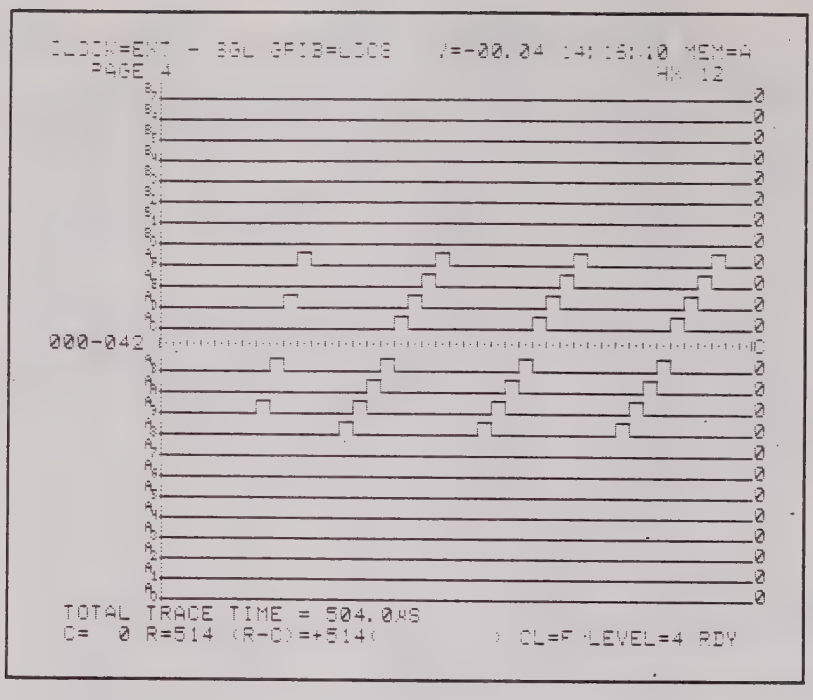

Figure 10-80. Four Pulses Sequence for Recording.

CLOCK=EXT - SGL GPIB=LOCS V=-00.04 14:16:10 MEM=A

	HH		HH		HH		HH		HH		HH
000	00	024	02	048	20	072	00	096	08	120	80
001	00	025	04	049	40	073	01	097	10	121	00
002	00	026	08	050	80	074	02	098	20	122	00
003	00	027	10	051	00	075	04	099	40	123	01
004	00	028	20	052	00	076	08	100	80	124	02
005	00	029	40	053	01	077	10	101	00	125	04
006	00	030	80	054	02	078	20	102	00	126	08
007	02	031	00	055	04	079	40	103	01	127	10
008	08	032	00	056	08	080	80	104	02	128	20
009	20	033	01	057	10	081	00	105	04	129	40
010	80	034	02	058	20	082	00	106	08	130	80
011	00	035	04	059	40	083	01	107	10	131	00
012	00	036	08	060	80	084	02	108	20	132	00
013	01	037	10	061	00	085	04	109	40	133	01
014	02	038	20	062	00	086	08	110	80	134	02
015	04	039	40	063	01	087	10	111	00	135	04
016	08	040	80	064	02	088	20	112	00	136	08
017	10	041	00	065	04	089	40	113	01	137	10
018	20	042	00	066	08	090	80	114	02	138	20
019	40	043	01	067	10	091	00	115	04	139	40
020	80	044	02	068	20	092	00	116	08	140	80
021	00	045	04	069	40	093	01	117	10	141	00
022	00	046	08	070	80	094	02	118	20	142	00
023	01	047	10	071	00	095	04	119	40	143	01

C= 10 R=514 (R-C)=+504( ) CL=F LEVEL=4 RDY

Figure 10-81. Trace on Four Levels Before Recording.

10.2.5.10 **Record, then Follow a Path**

SET UP: After capturing a memoryful of information, confirm that several subsequent words of the pattern occur in their proper sequence, i.e., 08, 20, then 80. See setup guide in Figure 10-82.

Press [TRACE CONTROL], [▷], twice, [V24 5 L], [Hx3 1 M], [V24 5 L], [▷], [Hx1 0 G], [▽ SET] three times, [Hx12 3 J], [▽ SET], [DON'T CARE *] [SPACE] twice, [▽ SET], [Hx3 1 M], [▽ SET], [Hx12 3 J], [▽ SET], [Hx1 0 G], [▽ SET], [PAGE↑ 8 O TTL], [Hx1 0 G], [▽ SET] twice, [Hx6 2 '].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [PAGE↓ 4 K], [EBCDIC 9 P ECL], [V12 6 M], [DATA].

Press [▷] slowly.

Note the cursor level at each location; this verifies the sequence of events that occurred after the main information was recorded (see Figure 10-83). After the information was recorded, subsequent words were checked to verify that the expected execution path occurred.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.7 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEGM.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AF AB
A T 2 AE AA
S 1 AD A9
LSB AC A8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each over —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = O
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count = Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count > = Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count < > Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS
TRACE EVERYTHING FOR 515 SAMPLES THEN ADVANCE.

LEVEL 1 (O-F) DELAY = _____ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 8

(0) TRACE IF DATA = T
T = 0 8

COMMENTS
WAIT FOR 08, TRACE IT AND ADVANCE

LEVEL 2 (O-F) DELAY = _____ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 2 0

(0) TRACE IF DATA = T
T = 2 0

COMMENTS
WAIT FOR 20, TRACE IT AND ADVANCE.

LEVEL 3 (O-F) DELAY = _____ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(0) STOP IF DATA = S
S = 8 0

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(0) TRACE IF DATA = T
T = 8 0

COMMENTS
WAIT FOR 80, TRACE IT AND STOP RECORDING

Figure 10-82. Setup Guide: Record, Then Follow a Path (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.7

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)
SECTION B = (_____●_____●_____) + (_____+_____+_____)
SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	DECIMAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SIGN Any radix, any sequence.
4	MIXED CF-A0 SIGN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached. OR DEVICE NOT AVAILABLE No RTE-816 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate. Section A + Section B + Section C + internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate. Section A + Section B + Section C + Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external clock sources.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 1 Ons. Section A, Section B, and/or Section C + Master (external) or internal clock period or 1 Ons.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 1 Ons. Section A, Section B, and/or Section C + Master (external) or internal or 1 Ons.
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 1 Ons. Section A, Section B, and or Section C + internal clock period or 1 Ons.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM CONDITION CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-82. Setup Guide: Record, Then Follow a Path (Sheet 2 of 2).

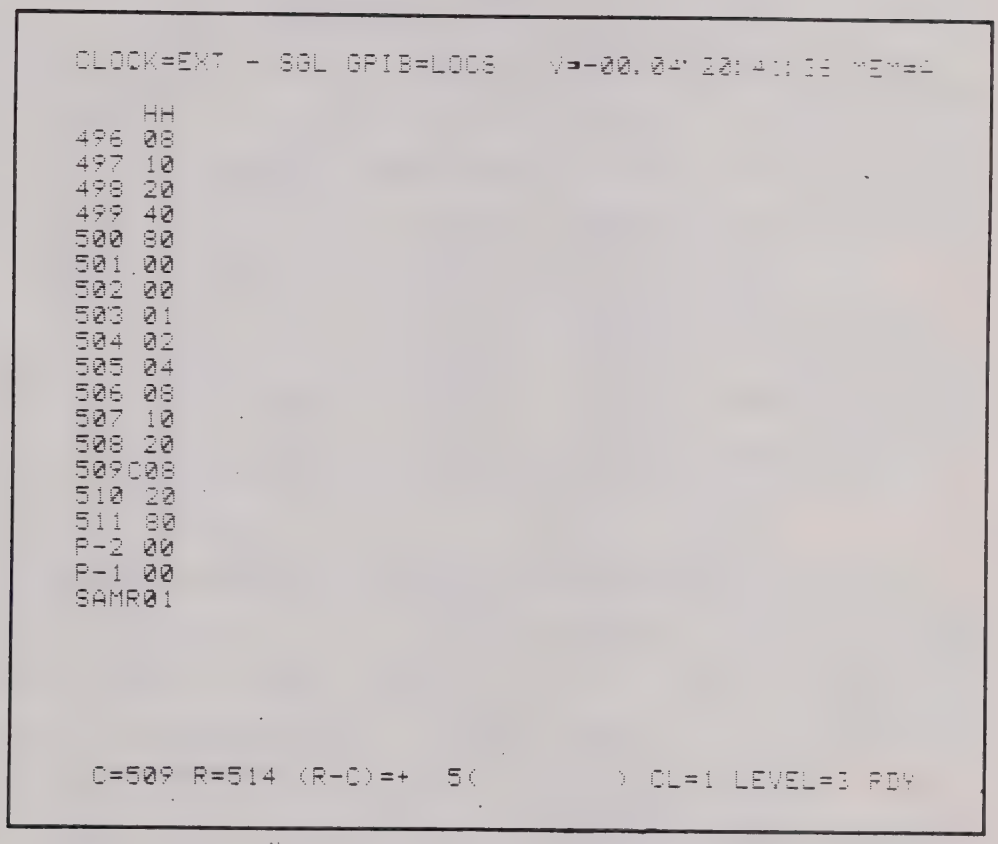

Figure 10-83. Verify Expected Execution Path.

10.2.5.11 **Check for Event 1 or Event 2**

SET UP: The place in the pattern cycle where the analyzer will begin sampling will vary with each recording. For example, if the first word sampled is 01, the next will be 02, the next 04, and so on; if the first word is 10, the next will be 20, the next 40, and so on. Therefore, one cannot predict whether 01 will appear before 10 or vice versa. The trace control program will end on level 1 if 10 occurs first and level 8 if 01 occurs first, thereby indicating exactly which happened when (see setup guide in Figure 10-84).

Press [TRACE CONTROL], [▽ SET], twice, [PAGE 8 TTL], [▷], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx1 0 G], [▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET] twice, [Hx3 1 H], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 H], [▽ SET], [PAGE 8 TTL], [▽ SET], [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Observe the trace level status field. It indicates which path was taken and therefore, which word occurred first. LEVEL = 1 RDY means 10 happened first. LEVEL = 8 RDY means 01 happened first.

Press [DATA] to verify.

Press [ARM] several times to see the varying end levels.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.8A OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AF AB
A T 2 AE AA
S 1 AD A9
LSB AC AB

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = 0
1	Always
2	Never
3	If DATA = 0 and Sample Count > Delay
4	If DATA = 0 and Sample Count < Delay
5	If DATA = 0 and Sample Count = Delay
6	If DATA = 0 and Sample Count > = Delay
7	If DATA = 0 and Sample Count < = Delay
8	If DATA = 0 and Sample Count < Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(0) JUMP TO 8 (O-F) IF DATA = J
J = 0 1
(0) ADVANCE IF DATA = A
A = 1 0
(1) TRACE ALWAYS
T = X X

COMMENTS
TRACE EVERYTHING WHILE LOOKING FOR 10 OR 01. IF 01 OCCURS 1st, GO TO LEVEL 8. OTHERWISE GO TO LEVEL 1.

LEVEL 1 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
THIS LEVEL IS ONLY ENTERED IF 10 OCCURED BEFORE 01. IT TRACES ONE SAMPLE AND STOPS.

LEVEL 8 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
THIS LEVEL IS ONLY ENTERED IF 01 OCCURED BEFORE 10. IT TRACES ONE SAMPLE AND STOPS.

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

QUICK KEY
(___) STOP
S =
(___) JUMP TO ___ (O-F)
J =
(___) ADVANCE
A =
(___) TRACE
T =

COMMENTS

Figure 10-84. Setup Guide: Check for Event 1 or Event 2 (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.8 A

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____ ● _____ ● AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = (_____ ● _____ ● _____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached. OR DEVICE NOT AVAILABLE No RTE-816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A Section B Section C & Master all can be different external expressions.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B, and or Section C - Master (external) or internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C - Master (external) or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C - internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-0.99 TO +4.99 VDC
B	VARB	-0.99 TO +0.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-84. Setup Guide: Check for Event 1 or Event 2 (Sheet 2 of 2).

10.2.5.12 **Take the Same Path Regardless of Which Event Occurred**

SET UP: As in paragraph 10.2.5.11, either 10 or 01 may be sampled first. Regardless, trace control goes to level 1 and stops. See setup guide in Figure 10-85.

Press [TRACE CONTROL] , [▽ SET] twice, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Press [SHIFT] , [◁ SET] , [V24 5 L] , [Hx1 0 G] , [Hx12 3 J] , [DATA] , [▷] seven times.

Your display should look like either Figure 10-86 or 10-87.

Press [ARM] repeatedly and observe the word in location 510. It may be 01 or 10, but tracing always stops at level 1.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.88 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB

I 6

D N 5

A P 4

T U 3 AEAB

A T 2 AEAA

S 1 ADA9

LSB ACAB

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count > = Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count < Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

QUICK KEY LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(0) JUMP TO 1 (O-F) IF DATA = J
J = 0 1

(0) ADVANCE IF DATA = A
A = 1 0

(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED WHILE LOOKING FOR EVENT 01 OR 10 TO OCCUR. REGARDLESS OF WHICH HAPPENS 1st, GO TO LEVEL 1.

QUICK KEY LEVEL 1 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE ONE SAMPLE AND STOP.

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(....) STOP
S =

(....) JUMP TO ___ (O-F)
J =

(....) ADVANCE
A =

(....) TRACE
T =

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(....) STOP
S =

(....) JUMP TO ___ (O-F)
J =

(....) ADVANCE
A =

(....) TRACE
T =

COMMENTS

Figure 10-85. Setup Guide: Take the Same Path Regardless of Which Event Occurred (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.8B

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR DEVICE NOT AVAILABLE No RTE-816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(→ — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A = Section B = Section C = internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B, and or Section C = Master/external or internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B, and or Section C = Master/external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A < B WITHIN LIMITS
5	AUTO STOP IF A > B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-85. Setup Guide: Take the Same Path Regardless of Which Event Occurred (Sheet 2 of 2).

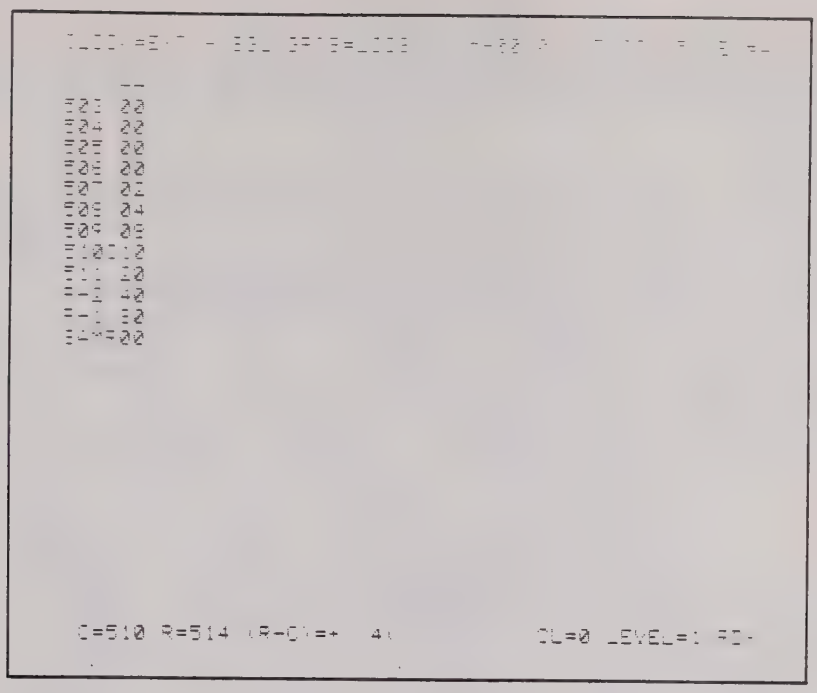


Figure 10-86. Sometimes 10 will occur on level 0.

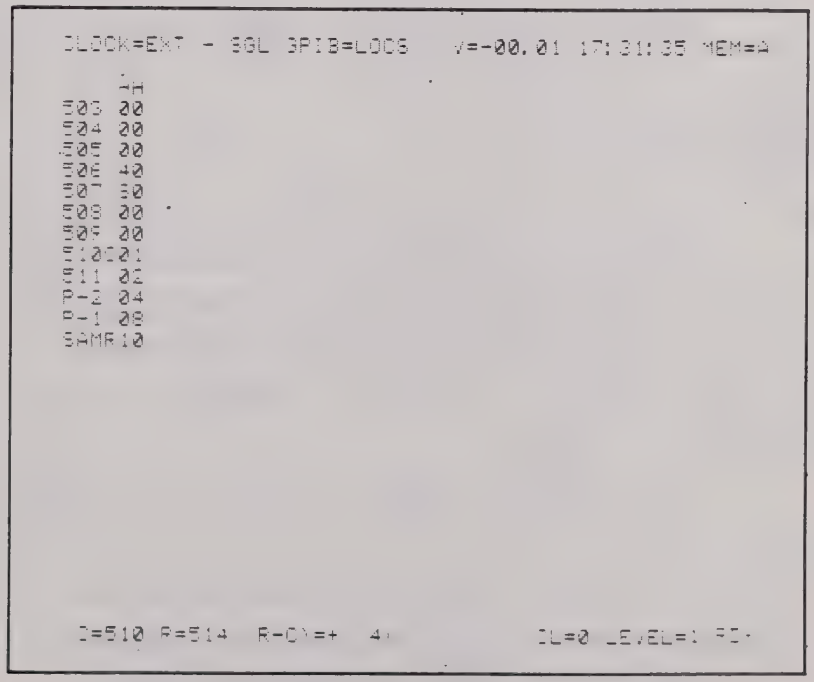


Figure 10-87. Sometimes 01 will occur on level 0.

10.2.5.13 **Check for Correct Timing Between Two Events**

SET UP: According to the Probe Test pattern there should be exactly four samples, or "ticks" of the master sample clock, between words 01 and 10. See setup guide in Figure 10-88 to verify this time interval.

Press [TRACE CONTROL], [▽ SET] twice, [▷], [Hx6 2 I], [▽ SET] twice, [Hx1 0 Q], [Hx3 1 M], [▽ SET] twice, [Hx3 1 M], [▷] twice, [Hx12 3 J], [▽ SET], [Hx6 2 I], [▽ SET], [PAGE 8 O TTL], [▷], [V6 7 N], [▽ SET], [Hx3 1 M], [Hx1 0 Q], [▽ SET], [Hx12 3 J], [▽ SET], [Hx3 1 M], [Hx1 0 Q], [▽ SET] twice, [Hx6 2 I], [▽ SET], [Hx3 1 M], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 M].

RECORD: Press [ARM].

REVIEW: Note that in the status field, tracing stopped at level 2 (2 RDY), indicating the time interval was correct (four or more sample clock pulses apart). There is no way to vary the actual time between the pulses; to simulate an incorrect time interval, change the delay on level 1 to four clocks.

Press [TRACE CONTROL], [Hx3 1 M], [▷] twice, [PAGE 4 K], [ARM].

Now notice that tracing stopped on level 8 because 10 came true at SAMPLE COUNT = 4 CLOCKS and therefore satisfied the JUMP condition of level 1.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #519 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AFAB
A T 2 AEAA
S 1 ADA9
LSB ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count > Delay
5	If DATA = D and Sample Count ≥ Delay
6	If DATA = D and Sample Count < Delay
7	If DATA = D and Sample Count ≠ Delay
8	If DATA = D and Sample Count = Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ ___ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE EVERYTHING WHILE LOOKING FOR 01. ADVANCE WHEN IT IS FOUND.

LEVEL 1 (O-F) DELAY = DEC 3 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(7) JUMP TO 8 (O-F) IF DATA = J AND SAMPLE COUNT < = DELAY
J = 1 0

(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = 1 0

(1) TRACE ALWAYS
T = X X

COMMENTS

EVENT 10 SHOULD OCCUR EXACTLY 4 CLOCKS AFTER ENTERING LEVEL 1 AND TRACE CONTROL THEREFORE ADVANCES TO LEVEL 2.

LEVEL 2 (O-F) DELAY = ___ ___ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

IF THE TIME BETWEEN 01 AND 10 WAS CORRECT, TRACING ADVANCES TO HERE AND STOPS.

LEVEL 8 (O-F) DELAY = ___ ___ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

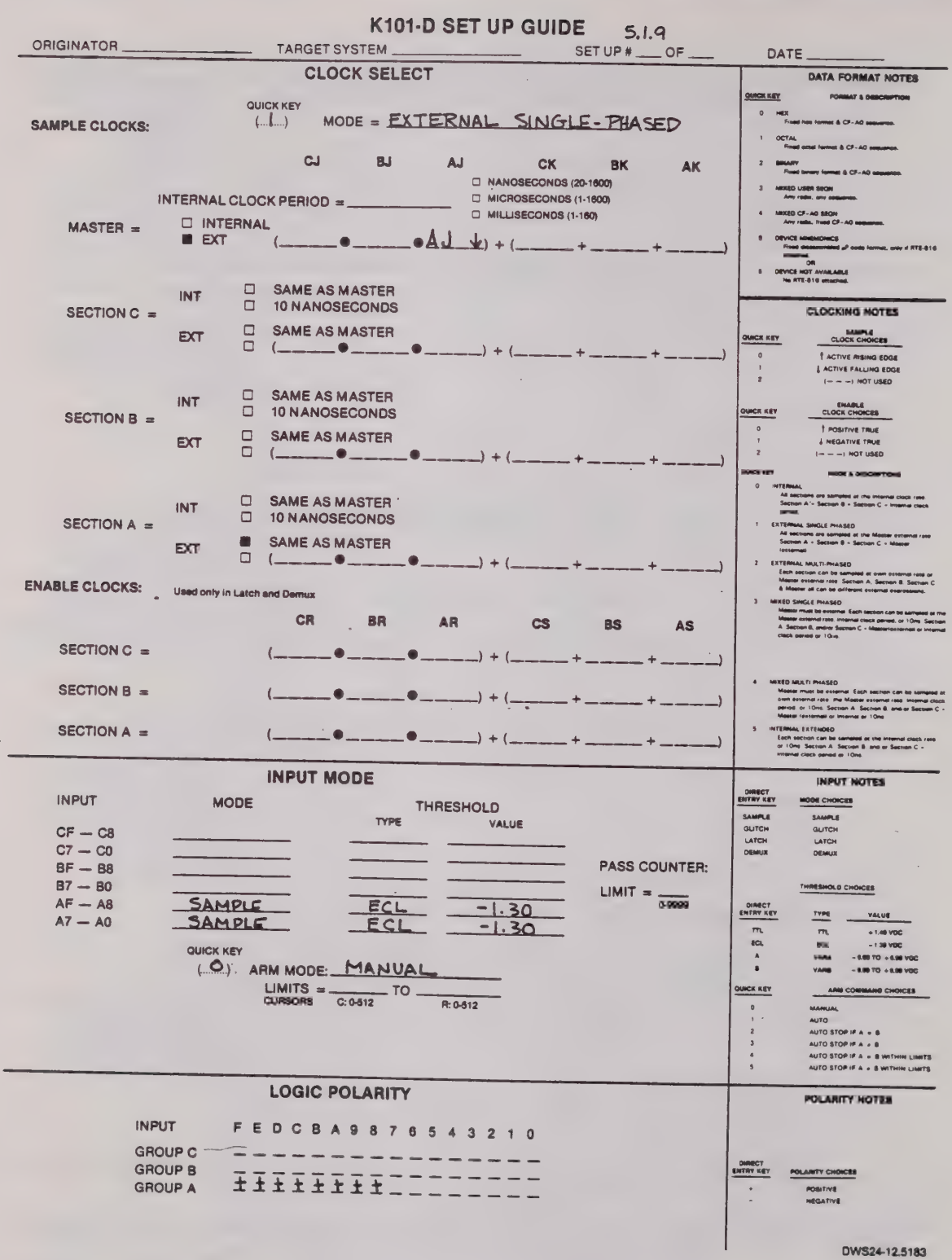
(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

IF THE TIME BETWEEN 01 AND 10 WAS INCORRECT TRACE CONTROL JUMPS TO HERE AND STOPS.

Figure 10-88. Setup Guide: Check Correct Timing Between Two Events (Sheet 1 of 2).



K101-D SET UP GUIDE 5.1.9

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)
SECTION B = (_____●_____●_____) + (_____ + _____ + _____)
SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
9	DEVICE MNEMONICS Fixed decade-coded μP code format, only if RTE-816 attached. OR
8	DEVICE NOT AVAILABLE No RTE-816 attached.

CLOCKING NOTES

SAMPLE CLOCK QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

ENABLE CLOCK QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

MODE QUICK KEY	MODE & DESCRIPTION
0	INTERNAL All sections are sampled at the internal clock rate. Section A + Section B + Section C + Internal clock period.
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate. Section A + Section B + Section C + Master (external)
2	EXTERNAL MULTI-PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external rates/periods.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (external) or internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B, and or Section C - Master (external) or internal or 10ns.
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and or Section C - internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-8.00 TO +8.00 VDC
B	VARB	-8.00 TO +8.00 VDC

ARM COMMAND QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	_	_	_	_	_	_	_	_	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	_	_	_	_	_	_	_	_

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

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Figure 10-88. Setup Guide: Check Correct Timing Between Two Events (Sheet 2 of 2).

10.2.5.14 Continuously Monitor for Correct Operation

a. Word 02

SET UP: To repeatedly check that word 02 occurs immediately after word 01, see setup guide in Figure 10-89.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 '], [▽ SET] twice, [Hx1 0 G], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx1 0 G], [▷], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx6 2 '], [▽ SET], [Hx1 0 G], [▽ SET], [DON'T CARE * SPACE] twice.

RECORD: Press [ARM].

REVIEW: Watch the trace level status field; it should alternate between 0 BUSY and 1 BUSY (the changing of the 0 and 1 may be difficult to detect). If and when an error occurs, it will go to 2 RDY. When it does,

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [Hx1 0 G], [DATA].

See Figure 10-90 for an example. In Figure 10-90 the word 02 should have occurred after word 01. Since it did not, tracing was halted. (The exact erroneous word will vary for each machine and recording, as well as the amount of elapsed time before an error occurs.)

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.10(1) OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

	MSB	
	I 6	
D	N 5	
A	P 4	
T	U 3	AFAB
A	T 2	AEAA
	S 1	ADA9
	LSB	ACA8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count = Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count = Delay
7	If DATA = D and Sample Count = Delay
8	If DATA = D and Sample Count = Delay

D = S, J, A, or T, which are assigned by command type.

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(0) TRACE IF DATA = T
T = 0 1

COMMENTS

WAIT FOR 01 - TRACE IT AND ADVANCE.

LEVEL 1 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(0) JUMP TO 0 (O-F) IF DATA = J
J = X X
(0) ADVANCE IF DATA = A
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS

EVENT 02 SHOULD OCCUR IMMEDIATELY UPON ENTERING LEVEL 1. IF SO, JUMP BACK. IF NOT, ADVANCE. TRACE THE EVENT THAT DOES OCCUR.

LEVEL 2 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE CONTROL COMES HERE AND STOPS ONLY IF 02 DID NOT OCCUR RIGHT AFTER 01.

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

QUICK KEY
(.....) STOP
S =
(.....) JUMP TO ___ (O-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

Figure 10-89. Setup Guide:Continuously Monitor for Correct Operation (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.10 (1)

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Preset hex format & CF-A0 sequence.
1	OCTAL Preset octal format & CF-A0 sequence.
2	BINARY Preset binary format & CF-A0 sequence.
3	MIXED USER SIGN Any radix, any sequence.
4	MIXED CF-A0 SIGN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Preset disassembled µP code format, only if RTE-816 attached. OR
6	DEVICE NOT AVAILABLE No RTE-816 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTION
0	INTERNAL All sections are sampled at the internal clock rate. Section A - Section B - Section C - Internal clock period.
1	EXTERNAL SINGLE-PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master reference.
2	EXTERNAL MULTI-PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master/external or Internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (external) or Internal or 10ns.
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and or Section C - Internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	_____	_____	_____
C7 — C0	_____	_____	_____
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

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Figure 10-89. Setup Guide:Continuously Monitor for Correct Operation (Sheet 2 of 2).

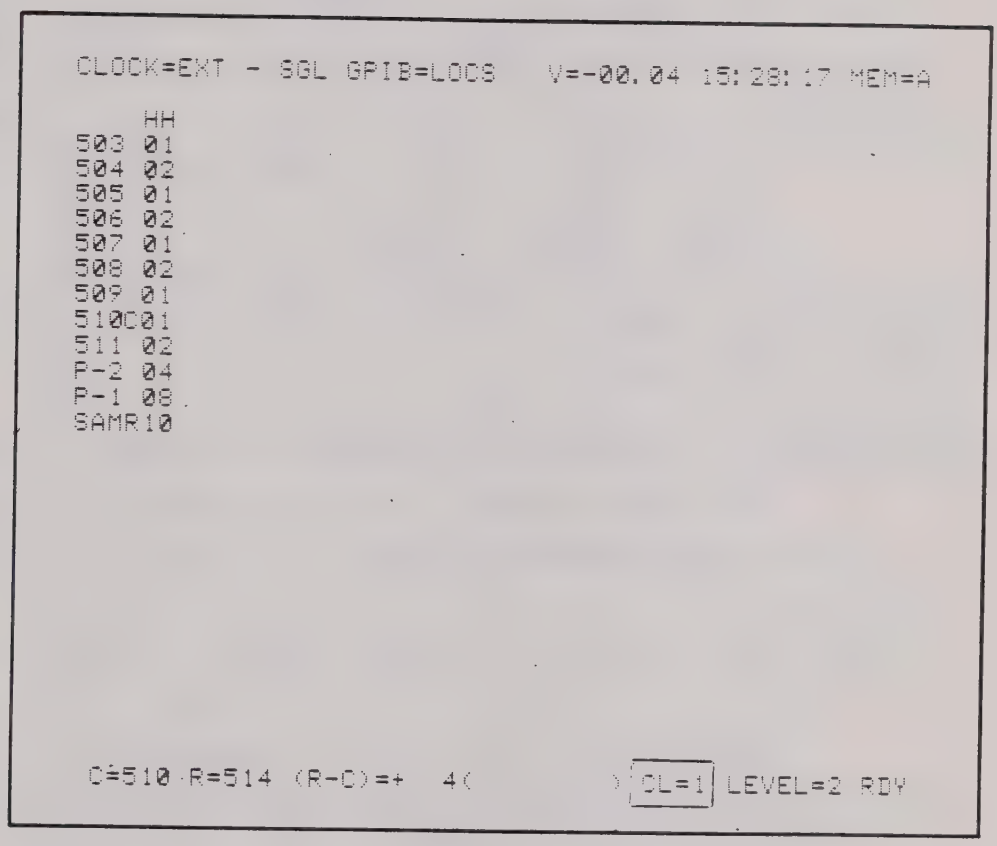


Figure 10-90. Tracing Halted.

b. Word 80

SET UP: To repeatedly check that word 80 occurs within the proper time interval (seven clocks) from the occurrence of 01, see setup guide in Figure 10-91.

Press [TRACE CONTROL], [Hx3 1 H], [▷], twice, [V6 7 N], [▽ SET], twice, [Hx1 0 G], [▷], [V6 7 N], [▽ SET], [PAGE 8 O TTL], [Hx1 0 G], [▽ SET], [Hx12 3 J].

RECORD: Press [ARM].

REVIEW: Watch the trace level status field. Again, it should toggle between 0 BUSY and 1 BUSY. If and when an error occurs, it will go to 2 RDY.

Press [DATA] to see the cause of the error, as in Figure 10-92. Because an extra sample (40) occurred between 01 and 80, the time interval between them was in error and tracing stopped.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST 5.1.10 (2) SET UP # ___ OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AEAB
A T 2 AEAA
S 1 ADA9
LSB AGA0

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count = Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count < = Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count < Delay

(D = 5 hex A or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S=X X
(2) JUMP TO 0 (0-F) NEVER
J=X X
(0) ADVANCE IF DATA = A
A=0 1
(0) TRACE IF DATA = T
T=0 1

COMMENTS
WAIT FOR 01, TRACE IT AND ADVANCE WHEN IT OCCURS.

LEVEL 1 (0-F) DELAY = DEC 7 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S=X X
(7) JUMP TO 0 (0-F) IF DATA = J AND SAMPLE COUNT < =DELAY
J=8 0
(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A=X X
(1) TRACE ALWAYS
T=X X

COMMENTS
EVENT 80 SHOULD OCCUR EXACTLY 7 CLOCKS AFTER EVENT 01. IF SO, JUMP BACK. IF NOT, ADVANCE, TRACE EVERYTHING THAT HAPPENS BETWEEN 01 AND 80.

LEVEL 2 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(1) STOP ALWAYS
S=X X
(2) JUMP TO 0 (0-F) NEVER
J=X X
(2) ADVANCE NEVER
A=X X
(1) TRACE ALWAYS
T=X X

COMMENTS
IF THIS LEVEL IS REACHED, A TIMING ERROR OCCURED.

STOP.

LEVEL ___ (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(____) STOP
S=
(____) JUMP TO ___ (0-F)
J=
(____) ADVANCE
A=
(____) TRACE
T=

COMMENTS

Figure 10-91. Setup Guide: Repeatedly Check Word 80 (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.10(2)

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal formats & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 emulator. OR
6	DEVICE NOT AVAILABLE No RTE 816 emulator.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTION
0	INTERNAL All sections are sampled at the internal clock rate. Section A + Section B + Section C = internal clock period.
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate. Section A + Section B + Section C = Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external frequencies.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 1/2ns. Section A, Section B, and/or Section C = Master (external) or internal clock period or 1/2ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 1/2ns. Section A, Section B, and/or Section C = Master (external) or internal or 1/2ns.
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 1/2ns. Section A, Section B, and or Section C = internal clock period or 1/2ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-91. Setup Guide: Repeatedly Check Word 80 (Sheet 2 of 2).

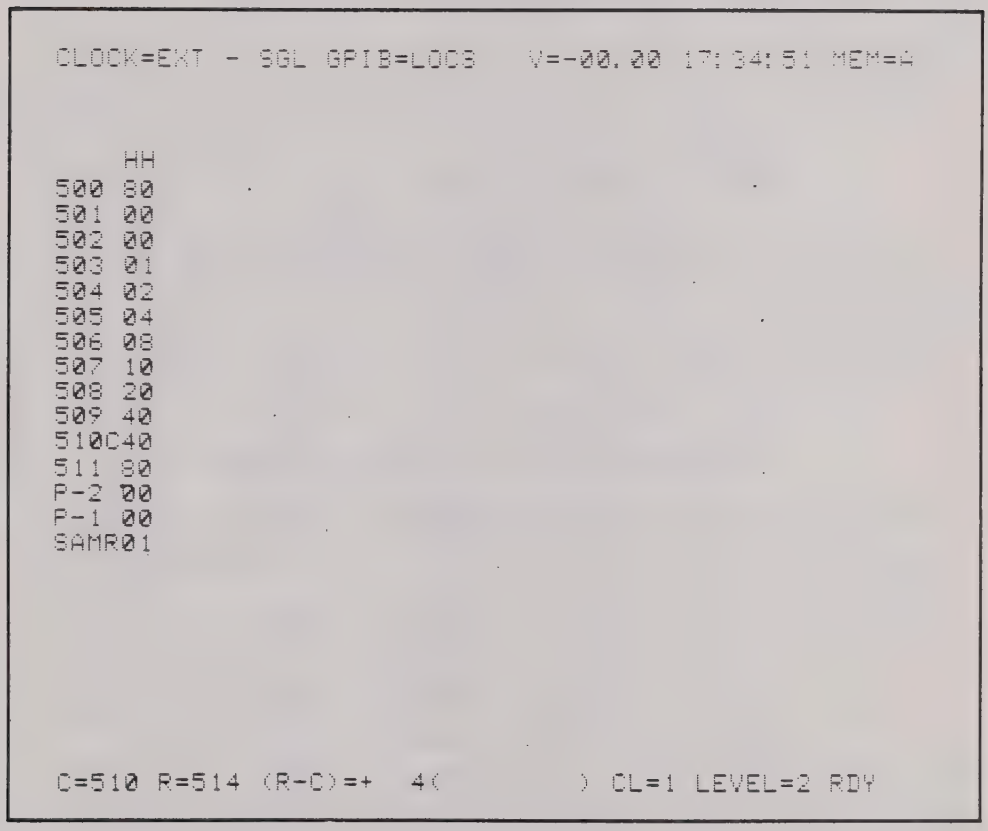


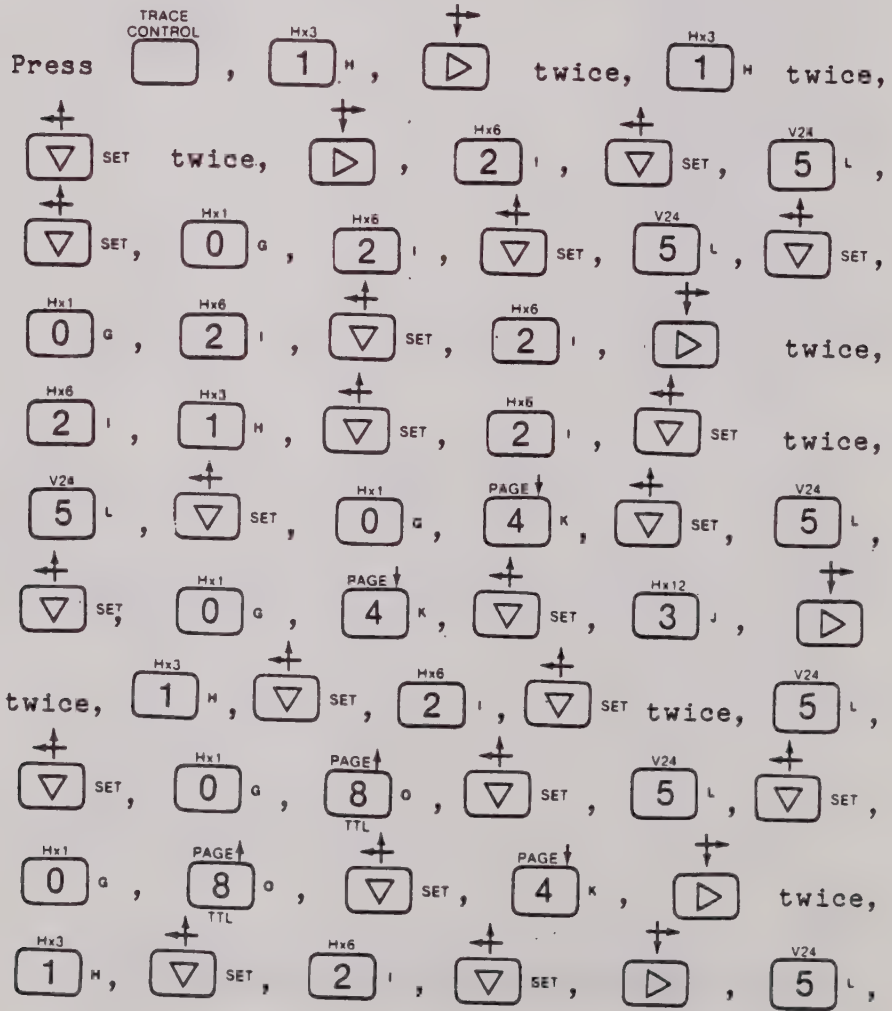
Figure 10-92. Time Interval Error, Tracing Stopped.

10.2.6 ADVANCED TRACE CONTROL

Combining and varying the basic building blocks let you create more complex and powerful trace control programs. The following examples will illustrate some of the more advanced trace control capabilities.

10.2.6.1 **Continuously Check Execution Path and Timing**

SET UP: To check that certain words occur in their expected sequence as well as within their expected time interval, see setup guide in Figure 10-93.



K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.2.1 OF ___ DATE _____

QUICK KEY (See back for notes) (.....) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
R P 4	
T U 3	$A_F A_E$
A T 2	$A_D A_C$
S 1	$A_B A_A$
LSB	$A_9 A_8$

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count > Delay
5	If DATA = D and Sample Count < Delay
6	If DATA ≠ D and Sample Count > = Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA ≠ D and Sample Count = Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) 0 (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO ___ (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS

BEGIN AT KNOWN STARTING POINT.

LEVEL 1 (O-F) DELAY = DEC (DEC/HEX) 11 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 2

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 2

COMMENTS

02 SHOULD OCCUR 1 CYCLE AND 1 WORD LATER.

LEVEL 2 (O-F) DELAY = DEC (DEC/HEX) 21 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 4

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 4

COMMENTS

04 SHOULD OCCUR 2 CYCLES AND 1 WORD LATER.

LEVEL 3 (O-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 8

(5) TRACE IF DATA = A AND SAMPLE COUNT = DELAY
T = 0 8

COMMENTS

08 IS NEXT IMMEDIATE WORD.

Figure 10-93. Setup Guide: Continuously Check Execution Path and Timing (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST (CONTINUED) SET UP # 5.2 J OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AE AB
A T 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = 0
1	Always
2	Never
3	If DATA = 0 and Sample Count > Delay
4	If DATA = 0 and Sample Count < Delay
5	If DATA = 0 and Sample Count = Delay
6	If DATA = 0 and Sample Count ≥ Delay
7	If DATA = 0 and Sample Count ≤ Delay
8	If DATA = 0 and Sample Count ≠ Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL 4 (O-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(5) JUMP TO 0 (O-F) IF DATA = J AND SAMPLE COUNT = DELAY
J = 1 0

(5) ADVANCE IF DATA = J AND SAMPLE COUNT = DELAY
A = X X

(0) TRACE IF DATA = T
T = 1 0

COMMENTS

BOTH JUMP AND ADVANCE ARE TRUE SIMULTANEOUSLY, BUT JUMP HAPPENS 1st, SO IT CONTINUOUSLY LOOPS BETWEEN LINK 0, 1, 2, 3, 4.

LEVEL 5 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

THIS LEVEL SHOULD NEVER BE REACHED.

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-93. Setup Guide: Continuously Check Execution Path and Timing (Sheet 2 of 2).

Press [▽ SET], [1 H], [0 Q], [▽ SET], [5 L], [▽ SET] twice, [0 Q], [▽ SET], [1 H], [0 Q].

RECORD: Press [ARM].

REVIEW: Watch the trace level status field continuously sequence through LEVEL = 0, 1, 2, 3, 4 BUSY as the conditions on each level are satisfied and the commands executed.

Note

If an error occurs in the generation or clocking of the Probe Test pattern, the trace program will get hung up (as indicated by a steady LEVEL = n BUSY) because the expected word on that level did not happen when it should have.

Press [M→A].

The recording will most likely stop on level 2 since more time is spent in that level than the others.

Press [SHIFT], [◁ SET], [5 L], [0 Q], [0 Q], [DATA].

Your display should look like Figure 10-94. The trace program repeatedly captures only one word on each of five levels until manually stopped.

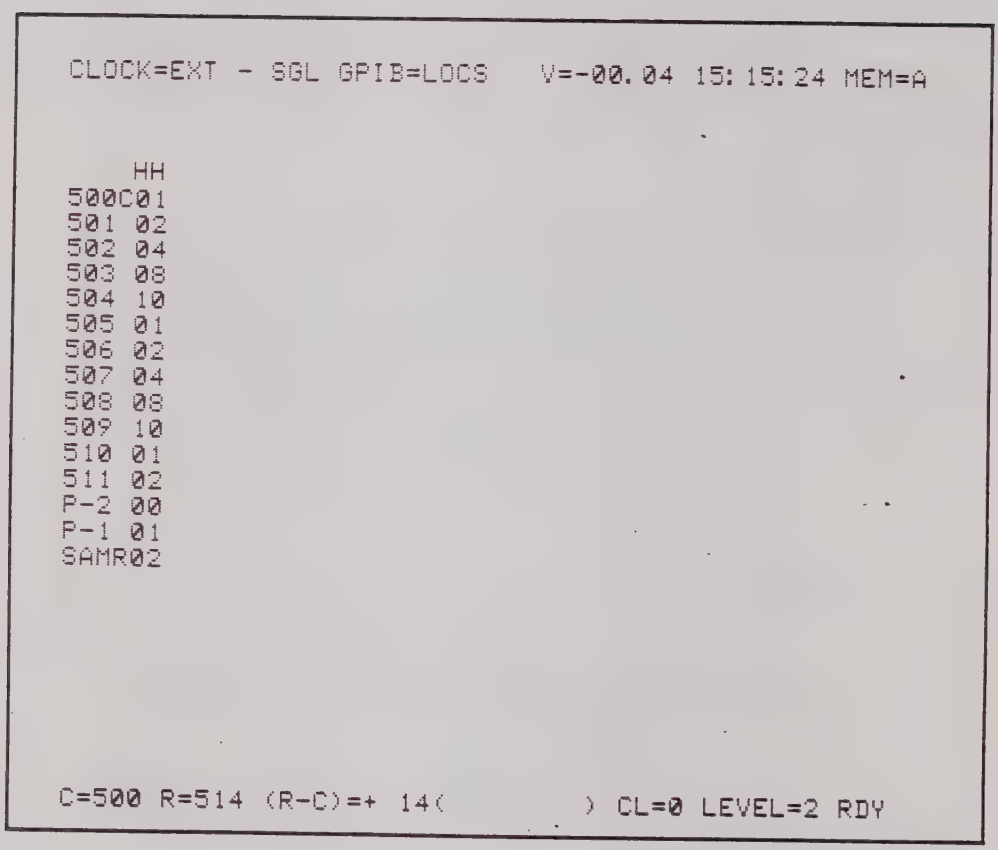


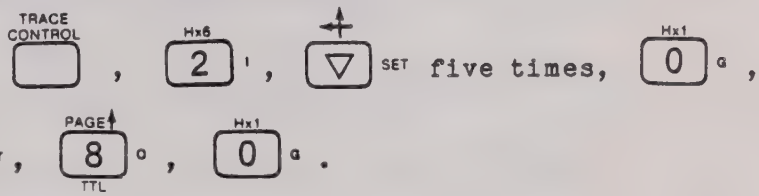
Figure 10-94. Capture One Word on Each Level until Stopped.

Press slowly and

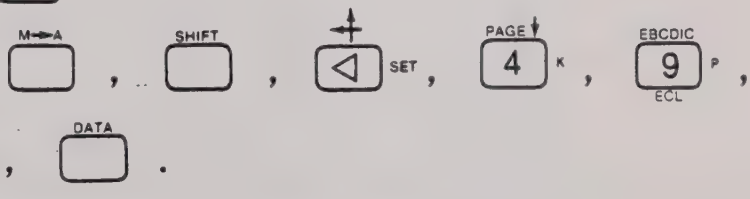
notice that 01 is captured by level 0; one cycle (ten sample clocks) and one sample later 02 is captured by level 1; two cycles and one sample later 04 is captured by level 2; one sample later 08 is captured by level 3; one sample later 10 is captured by level 4; then the whole process repeats. Figure 10-95 shows the exact words that were traced by this program out of all the words that were sampled. Note that of all the samples being evaluated by trace control, only certain samples will be transferred into memory.

10.2.6.2 **Trace Independently of the Execution Path**

SET UP: Change the trace control setup on level 2.

Press 

RECORD: Press

REVIEW: Press 

Your display will look similar to Figure 10-96. Taking the same execution path as before, different samples are selected to be recorded.

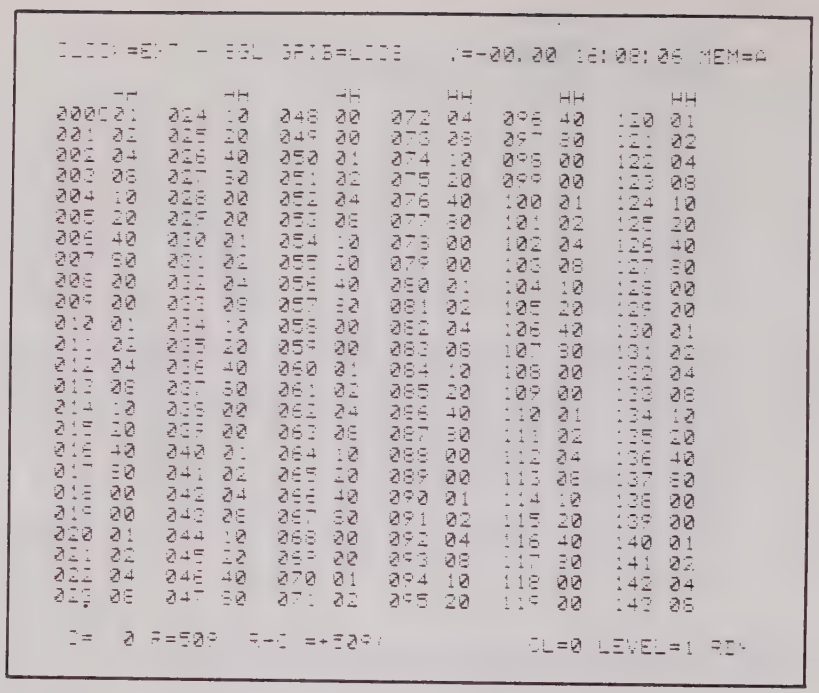


Figure 10-95. Transfer Certain Samples into Memory.

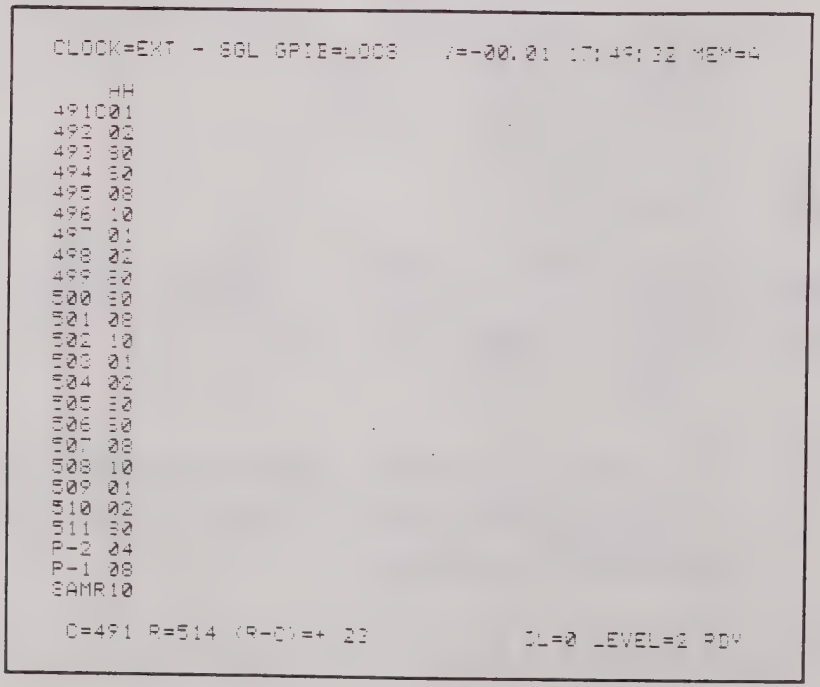


Figure 10-96. Changing Sample Selection.

Press [▷] until CL = 2.

Level 2 still checks for and advances on the second occurrence of 04, but it now traces the two occurrences of 80 that happen while waiting for ADVANCE to come true (see Figure 10-97). While waiting for the level 2 ADVANCE condition to come true, two occurrences of 80 are traced. The TRACE command and its T word recognizer do not have to be the same as any of the other commands and their word recognizers. The words you choose to record don't have to be the same as the words that define the execution path to be followed.

10.2.6.3 **End Level Breakpoint**

SET UP: Change the trace control program end level to 3.

Press [TRACE CONTROL] , [◁ SET] , [Hx12 3] .

Press [▷] , then [CHOICE NEXT] repeatedly to verify that the end level you set applies to all 16 levels.

RECORD: Press [ARM] .

REVIEW: Press [DATA] , and use [▷] to move the Control Cursor to location 511 (Figure 10-98). Note that though the last sample traced occurred in level 3, end level 3 forces an advance to level 4 and stops the recording there.

Note that the last word was traced by level 3 (CL = 3) and the recording stopped on level 4 (LEVEL = 4 RDY), although none of the level 4 commands were performed. Setting end level to n (where n is a level used in the current program) causes trace control to advance to level

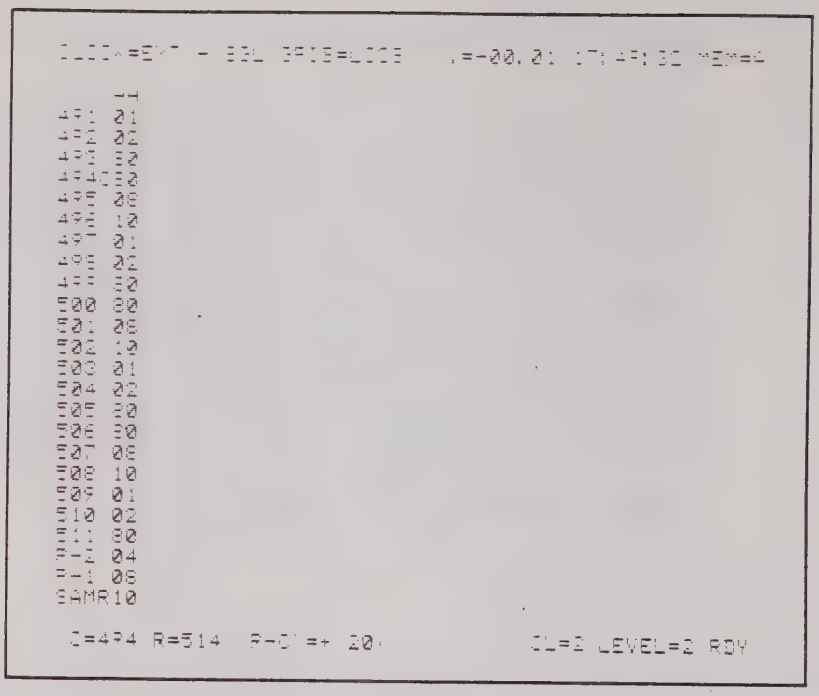


Figure 10-97. Record While Waiting.

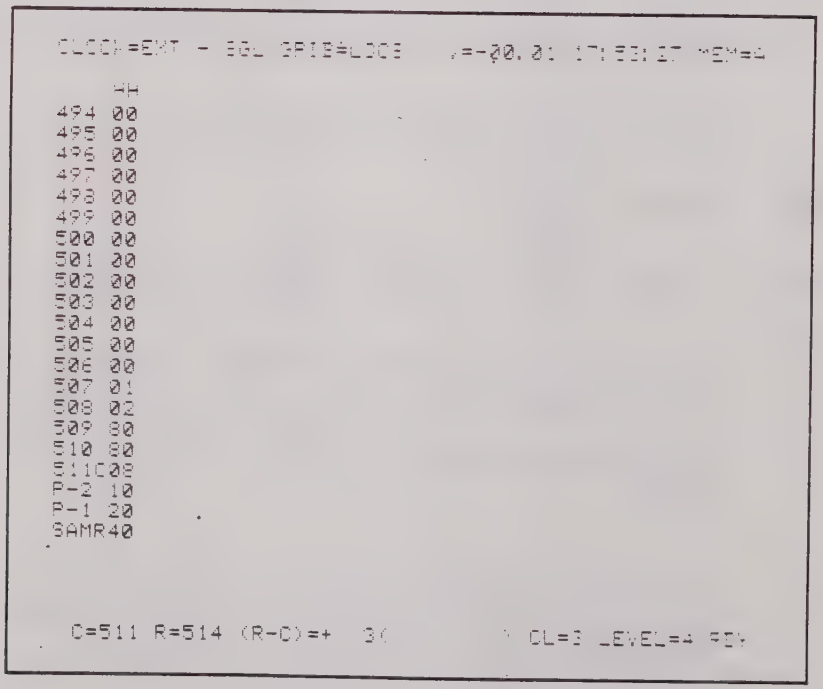


Figure 10-98. End Level 3 Forces.

n + 1, regardless of the commands on level n, and stop on level n + 1 without performing any of the commands on n + 1. In this way, end level can be used as a breakpoint to check out segments of your trace control program.

10.2.6.4 **Segments, Patterns, and Total Trace Time**

SET UP: See setup guide in Figure 10-99.

Press [TRACE CONTROL], [Hx3 1 M], [▷], twice, [V12 6 M], [V24 5 L], [Hx1 0 G], [Hx1 0 G], [Hx1 0 G], [▷], [Hx3 1 M], [▷], [DEMUX HEX F V], [▷], [Hx6 2 I], [▷], twice, [Hx3 1 M], [Hx1 0 G], [Hx3 1 M], [▽ SET] five times, [Hx6 2 I], [▽ SET], [Hx12 3 J], [▽ SET], [Hx3 1 M].

RECORD: Press [ARM].

REVIEW: Notice that the trace level status word remains at 1 BUSY for a moment before going to 3 RDY.

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [V24 5 L], [Hx3 1 M], [▷] six times.

Your display should look like Figure 10-100.

Press [TIMING] and note the total trace time of 2 micro-seconds. This is because trace control was only enabled to record one word on levels 0, 1, and 2. Change trace control to trace every occurrence of the level 2 A pattern.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.24 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AFA8
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count > = Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count < > Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS
WAIT FOR 0.1, TRACE IT AND ADVANCE WHEN IT OCCURS.

LEVEL 1 (O-F) DELAY = DEC 65000 (DEC/HEX) (0-65 K) A PATTERNS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 2

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 2

COMMENTS
WAIT FOR THE 65000 TH OCCURANCE OF EVENT 02. TRACE ONLY THAT LAST OCCURANCE AND THEN ADVANCE.

LEVEL 2 (O-F) DELAY = DEC 101 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 4

(2) TRACE NEVER
T = 0 4

COMMENTS
DON'T TRACE ANYTHING WHILE CHECKING FOR EVENT 04 WHICH SHOULD OCCUR EXACTLY 101 CLOCKS AFTER LEAVING THE LAST LEVEL.

LEVEL 3 (O-F) DELAY = DEC 1 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 8

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 8

COMMENTS
CHECK THAT EVENT 08 OCCURS IMMEDIATELY UPON ENTERING THIS LEVEL. IF IT DOES, TRACE IT. STOP RECORDING. THE ADVANCE COMMAND SHOULD NOT BE EXECUTED WHEN IT COMES TRUE AS STOP TAKES PRIORITY.

Figure 10-99. Setup Guide: Segments, Patterns, and Total Trace Time (Sheet 1 of 2).

K101-D SET UP GUIDE 5.2.4

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)
SECTION B = (_____●_____●_____) + (_____+_____+_____)
SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SEQN Any radix, any sequence.
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled 8P code format, only if RTE-816 attached OR DEVICE NOT AVAILABLE No RTE-816 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate. Section A = Section B = Section C = internal clock period.

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate. Section A = Section B = Section C = Master (external).

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or internal clock period or 10ns.

4 MIXED MULTI PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or internal or 10ns.

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and/or Section C = internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL
LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-5.00 TO +5.00 VDC
B	VARB	-5.00 TO +5.00 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	+	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-99. Setup Guide: Segments, Patterns, and Total Trace Time (Sheet 2 of 2).

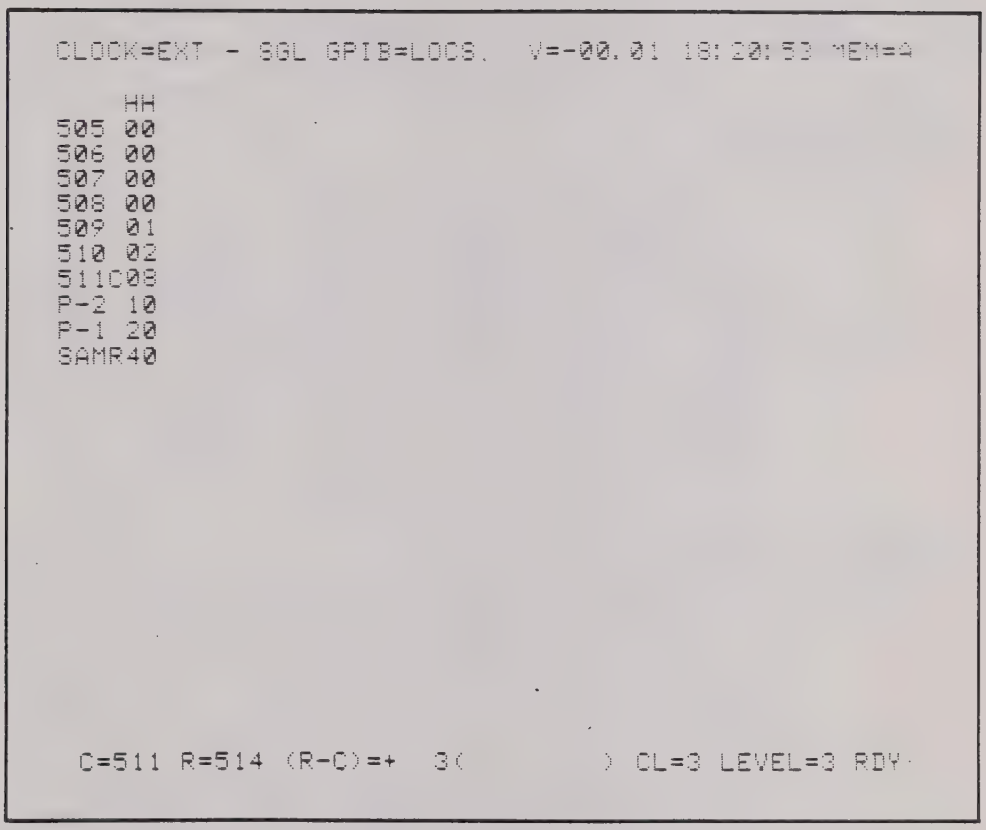

Figure 10-100. Only Three Words are Traced into Memory.

Press [TRACE CONTROL] , [Hx3 1 H] , [SET ▽] five times, [Hx1 0 G] .

Press [ARM] , [TIMING] .

Note that the total trace time is now (typically) 65.26 milliseconds.

10.2.7 RECORD

10.2.7.1 Manual Arm

SET UP: See setup guide in Figure 10-101.

Press [TRACE CONTROL] , [SET ▽] , [Hx12 3 J] , [SET ▽] , [Hx1 0 G] , [Hx3 1 H] , [SET ▽] twice, [Hx6 2 I] , [SET ▽] twice, [Hx3 1 H] , [INPUT MODE] , [△] twice, [▷] , [PAGE 8 O TTL] .

RECORD: Press [ARM] .

The instrument makes a single recording for each manual press of [ARM] . This allows you to take all the time you need to review and analyze each recording.

REVIEW: Press [SHIFT] , [SET ◁] , [Hx1 0 G] , [TIMING] , [Hx12 3 J] (and [PAGE 4 K] or [PAGE 8 O TTL] as necessary to be on Page 4).

Your display should look like Figure 10-102 which is a timing display of a Probe Test recording. Manual recording allows unlimited time to review and analyze a display.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 6.1 OF ___ DATE _____

QUICK KEY (Also back for reset) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AFAB
A T 2	AEAA
S 1	ADA9
LSB	AGA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level in TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = O
1	Always
2	Never
3	If DATA = O and Sample Count > Delay
4	If DATA = O and Sample Count = Delay
5	If DATA = O and Sample Count < Delay
6	If DATA = O and Sample Count ≥ Delay
7	If DATA = O and Sample Count ≤ Delay
8	If DATA = O and Sample Count ≠ Delay

(O = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

FILL MEMORY AND STOP THE NEXT TIME 0.1 OCCURS.

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP
S =

(___) JUMP TO ___ (O-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP
S =

(___) JUMP TO ___ (O-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP
S =

(___) JUMP TO ___ (O-F)
J =

(___) ADVANCE
A =

(___) TRACE
T =

COMMENTS

Figure 10-101. Setup Guide: Manual Arm (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # 6.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXT. SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence.
2	BINARY Fixed binary format & CF-A0 sequence.
3	MIXED USER SIGN Any radix, any sequence.
4	MIXED CF-A0 SIGN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembling µP code format, only if RTE-816 attached. OR
5	DEVICE NOT AVAILABLE No RTE-816 attached.

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A + Section B + Section C + Internal clock period
1	EXTERNAL SINGLE-PHASED All sections are sampled at the Master external rate Section A + Section B + Section C + Master restemal
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 1Ons. Section A, Section B, and/or Section C - Masterrestemal or internal clock period or 1Ons
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 1Ons. Section A, Section B, and/or Section C - Master restemal or internal or 1Ons
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 1Ons. Section A, Section B, and/or Section C - Internal clock period or 1Ons

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ___ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

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Figure 10-101. Setup Guide: Manual Arm (Sheet 2 of 2).

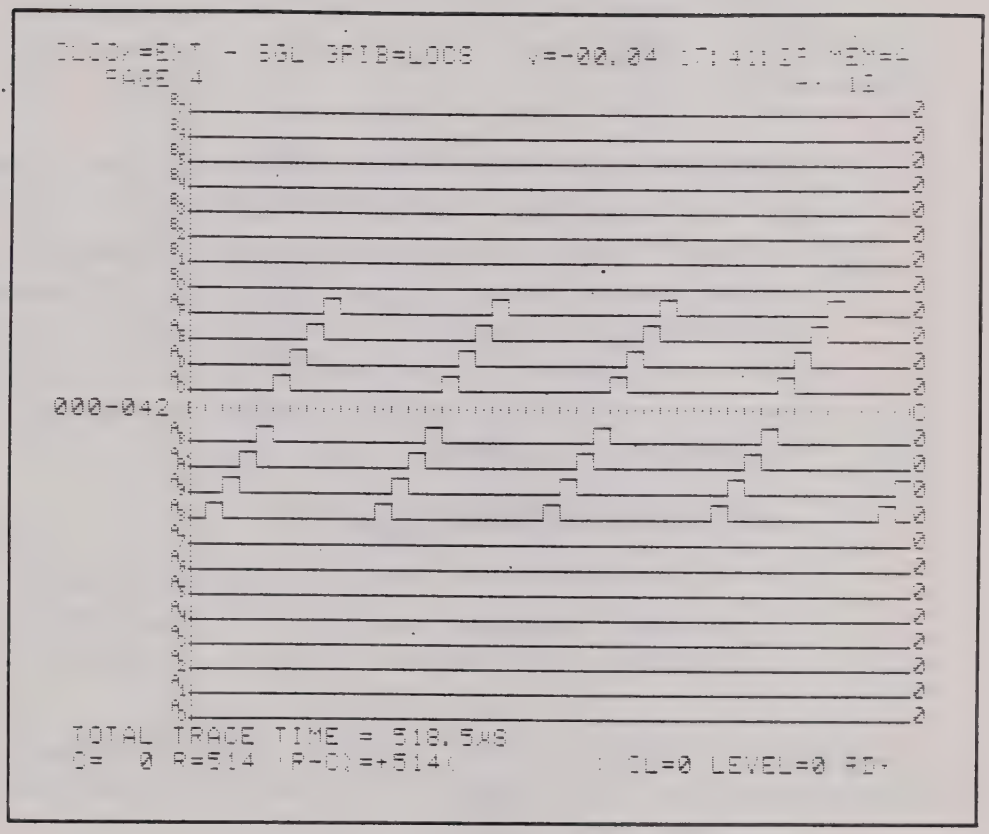


Figure 10-102. Probe Test Timing Display.

10.2.7.2 **Auto Arm**

SET UP: To avoid repeatedly pressing [ARM] by hand when you need to make multiple recordings, change the arm mode to Auto.

Press [INPUT MODE] , [△] , [Hx3 1 H] .

RECORD: Press [ARM] .

Watch the trace control level and status words. LEVEL = alternates between * and 0. The current trace level and number of the current recording are indicated in the bottom status field. A cumulative count of completed recordings is displayed in the upper right of the Input Mode screen (see Figure 10-103). While this automatic rearming and recording process is going on you can press any DISPLAY or SPECIFY key at any time.

Note

It is possible to change a setup parameter of Specify screen during auto recordings. However, to ensure that the change is accepted, press [STOP] , make the change, then press [ARM] .

Press [DATA] , [TIMING] , [GRAPH] .

Observe several recording cycles in each display mode. Press the other DISPLAY keys to see their effect.

This process can continue indefinitely as long as the trace control conditions of each recording are satisfied. If an expected STOP, JUMP, or ADVANCE command condition

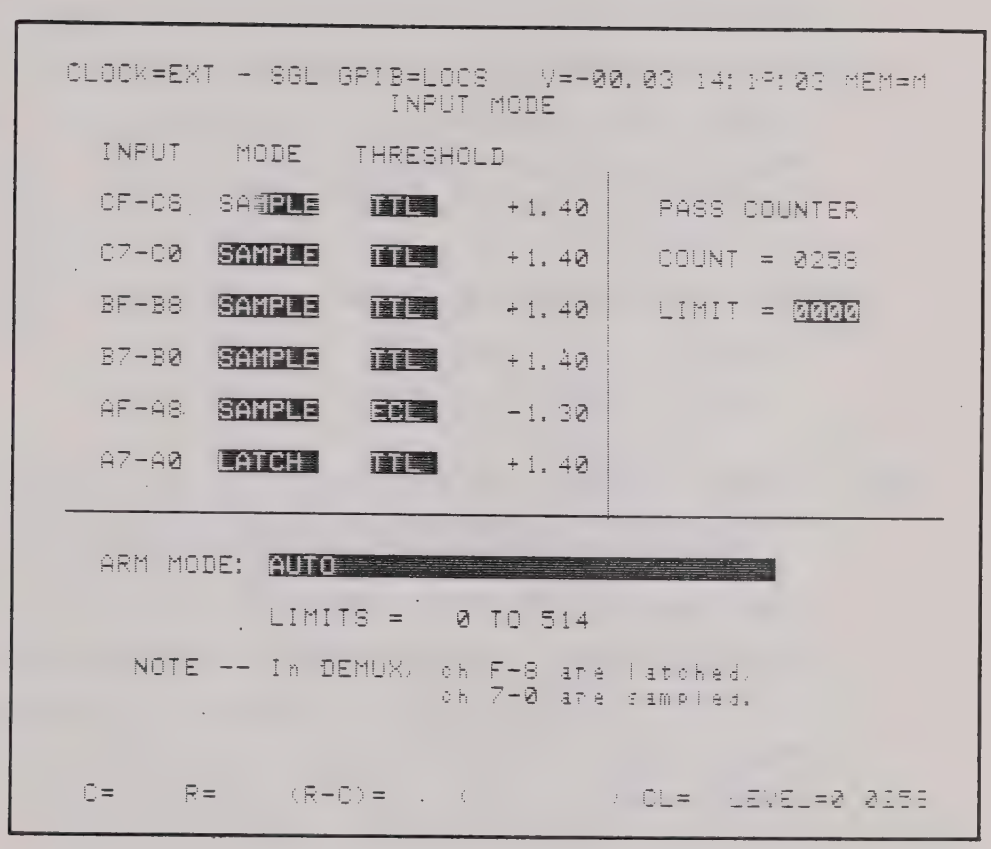


Figure 10-103. Status Field Display.

is not met, the process stops. The level message displays the number of the "stuck" trace level and the count stays at the count of the current hung up recording. If and when the condition comes true, the auto arming and count resume where they left off. Similarly, loss of an external clock input causes a halt. To simulate such an error, unplug the probe from the test socket. Note that the trace status says F CLK? because the expected external sample clock is absent. Plug the probe back in. The recordings and count will resume.

To completely halt the process you must press [STOP] or [M→A]. Press [STOP].

REVIEW: Notice that the trace status word has gone to RDY. The total number of recordings you made can be seen by pressing **INPUT MODE** (see Figure 10-104). The trace status word RDY indicates the completion of an auto arming recording cycle. The total number of recordings made is held until a new arm cycle is begun. If you press **ARM** again, the count initializes to zero and the process begins again.

10.2.7.3 **Limiting the Count**

SET UP: Set a limit of 100 cycles.

Press [INPUT MODE], [▷] twice, [1]^{Hx3}, [0]^{Hx1} twice.

Setting a limit on the pass counter stops automatic recordings when that limit is reached. If all 100 recordings are successful (i.e., do not fail or get hung up) then you can be reasonably confident your system will not fail more than 1 time out of 100. Confidence that

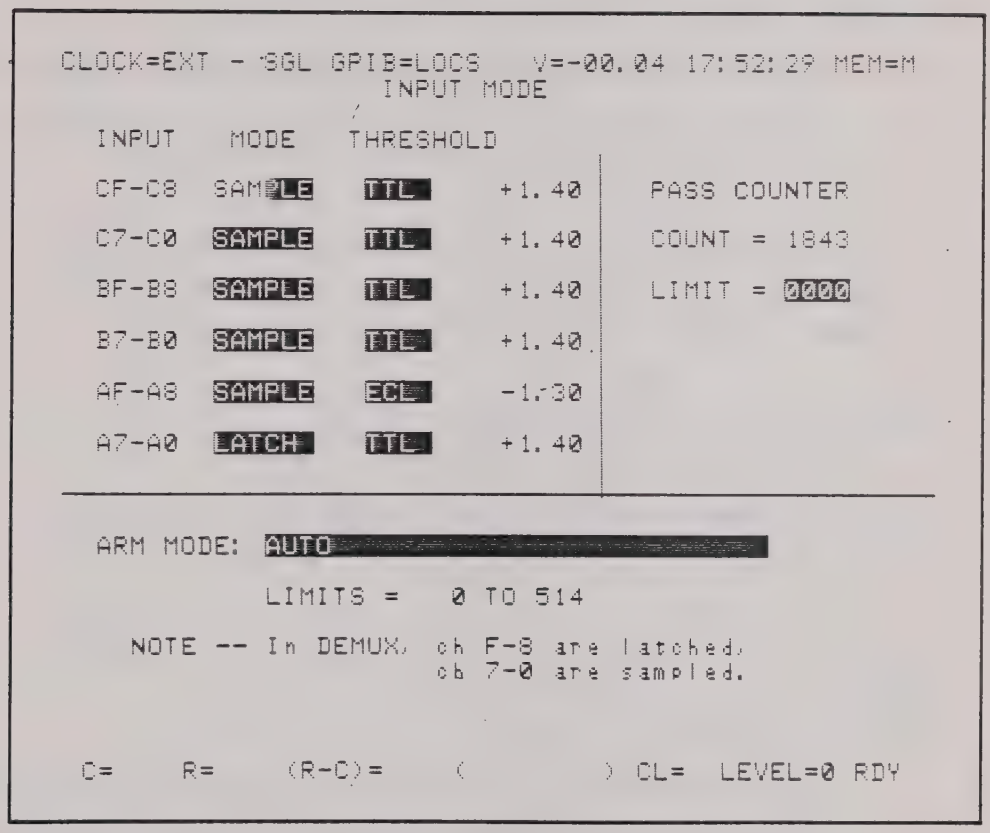


Figure 10-104. Completion of Auto Arming Recording Cycle.

your system is truly operational and debugged comes from obtaining successful test results over numerous recordings.

RECORD: Press [ARM] and observe the count.

It continues until 100 recordings have been made and then stops (see Figure 10-104a and 10-104b) as long as each test is successful. Remove the count limit.

Press [INPUT MODE], [▷] twice, [Hx1 0] G.

10.2.7.4 **Stop if A ≠ B**

SET UP: Press [INPUT MODE], [△], [Hx12 3] J.

To load memory B with a known "good" recording, press [A→B].

RECORD: Press [ARM].

New recordings are continually compared to the contents of B in search of any unknown or intermittent errors. This process is sometimes referred to as "baby-sitting." Observe the count. To create an "error" or difference between the current and stored recording, edit the B memory.

Press [DATA], [B], [EDIT], [▽] SET, [Hx3 1] H, [EDIT].

The process stops since A and B are now unequal.

REVIEW: Press [COMPARE A/B] .

The display should look like Figure 10-105. Any difference between the current and reference recording will stop the automatic arming process. To see the number of recordings and comparisons made before the "error" occurred,

press [INPUT MODE] .

ALTERNATE

SET UP: An alternate method of comparing recordings is to change Clock Select display to the following:

MODE = INTERNAL

INTERNAL CLOCK PERIOD = 40 NANOSECONDS

Press [CLOCK SELECT] , [Hx1 0 G] , [▽ SET] , [PAGE 4 K] , [Hx1 0 G] .

RECORD: Press [ARM] .

The instrument will make one recording and stop. Press [A→B] to load memory B.

Press [ARM] again.

Even though the trace control routine is identical, samples are now being taken asynchronously. It is therefore unlikely that every sample will be taken at exactly the same place in the pattern as in the previous recording. Therefore, auto arming will probably stop after only one recording.

```
CLOCK=EXT - SGL GPIB=LOCS   V=-00.03 16:21:19 MEM=B

    HH       HH       HH       HH       HH       HH
000C00  024 08  048 80  072 02  096 20  120 00
001≠11  025 10  049 00  073 04  097 40  121 01
002 02  026 20  050 00  074 08  098 80  122 02
003 04  027 40  051 01  075 10  099 00  123 04
004 08  028 80  052 02  076 20  100 00  124 08
005 10  029 00  053 04  077 40  101 01  125 10
006 20  030 00  054 08  078 80  102 02  126 20
007 40  031 01  055 10  079 00  103 04  127 40
008 80  032 02  056 20  080 00  104 08  128 80
009 00  033 04  057 40  081 01  105 10  129 00
010 00  034 08  058 80  082 02  106 20  130 00
011 01  035 10  059 00  083 04  107 40  131 01
012 02  036 20  060 00  084 08  108 80  132 02
013 04  037 40  061 01  085 10  109 00  133 04
014 08  038 80  062 02  086 20  110 00  134 08
015 10  039 00  063 04  087 40  111 01  135 10
016 20  040 00  064 08  088 80  112 02  136 20
017 40  041 01  065 10  089 00  113 04  137 40
018 80  042 02  066 20  090 00  114 08  138 80
019 00  043 04  067 40  091 01  115 10  139 00
020 00  044 08  068 80  092 02  116 20  140 00
021 01  045 10  069 00  093 04  117 40  141 01
022 02  046 20  070 00  094 08  118 80  142 02
023 04  047 40  071 01  095 10  119 00  143 04
   TOTAL ≠ =   1     FIRST ≠ =   1     LAST ≠ =   1
 C=   0 R=514 (R-C)=+514(     .     ) CL=0 LEVEL=0 RDY
```

Figure 10-105. Automatic Arming Process Stopped.

REVIEW: Press DATA to see the specific differences.

There may be a few differences (see Figure 10-106) or many (see Figure 10-107). Figure 10-106 shows that even similarly traced asynchronous recordings usually differ due to the one sample uncertainty of plus or minus one. Figure 10-107 shows that similarly traced asynchronous recordings may differ significantly depending on the specified sample rate and trace condition.

Press ARM several times.

10.2.7.5 **Auto Stop if A = B**

SET UP: To check for a specific suspected error, or to check if and when a system will perform as specifically desired, change the arm mode to look for equality.

Press INPUT MODE , △ , Hx6 2 .

RECORD: Press ARM .

Watch the count. Because of the asynchronous sampling, each new recording will most likely be different from the stored recording. However, the odds are good that eventually an exact match will occur and therefore halt the process. In Figure 10-108 267 asynchronous recordings were taken and compared before a match occurred.

REVIEW: When rearming stops, press DATA .

Note that the memory contents are identical. In Figure 10-109 every sample of the 267th recording is identical to the previously stored recording.

```
CLOCK=0040 nSEC GPIB=LOCS   V=-00.03 16:36:51 MEM=A

    HH      HH      HH      HH      HH      HH
000C00  024 01  048 02  072 04  096 08  120 10
001 00  025 01  049 02  073 04  097 08  121 10
002 00  026 01  050 02  074 04  098 08  122 10
003 00  027 01  051 02  075 04  099 08  123 10
004 00  028 01  052 02  076 04  100 08  124 10
005 00  029 01  053 02  077 04  101 08  125 10
006 00  030 01  054 02  078 04  102 08  126 10
007 00  031 01  055 02  079 04  103 08  127 10
008 00  032 01  056 02  080 04  104 08  128 10
009 00  033 00  057 02  081 04  105 08  129 10
010 00  034 02  058 00  082 04  106 08  130 10
011 01  035 02  059 00  083 00  107 08  131 10
012 01  036 02  060 04  084 08  108 00  132 10
013 01  037 02  061 04  085 08  109 00  133*10
014 01  038 02  062 04  086 08  110 00  134 20
015 01  039 02  063 04  087 08  111 10  135 20
016 01  040 02  064 04  088 08  112 10  136 20
017 01  041 02  065 04  089 08  113 10  137 20
018 01  042 02  066 04  090 08  114 10  138 20
019 01  043 02  067 04  091 08  115 10  139 20
020 01  044 02  068 04  092 08  116 10  140 20
021 01  045 02  069 04  093 08  117 10  141 20
022 01  046 02  070 04  094 08  118 10  142 20
023 01  047 02  071 04  095 08  119 10  143 20
    TOTAL * =  2    FIRST * =133    LAST * =383
 C=  0 R=514 (R-C)=+514( 20.56nS) CL=0 LEVEL=0 RDY
```

Figure 10-106. Asynchronous Recordings Differences.

```
CLOCK=0040 nSEC GPIB=LOCS   V=-00.03 16:39:05 MEM=A

    HH      HH      HH      HH      HH      HH
000C01  024*02  048*04  072*08  096*10  120*20
001*01  025*02  049*04  073*08  097*10  121*20
002*01  026*02  050*04  074*08  098*10  122*20
003*01  027*02  051*04  075*08  099*10  123*20
004*01  028*02  052*04  076*08  100*10  124*20
005*01  029*02  053*04  077*08  101*10  125*20
006*01  030*02  054*04  078*08  102*10  126*20
007*01  031*02  055*04  079*08  103*10  127*20
008*01  032*02  056*04  080*08  104*10  128*20
009*01  033*02  057*04  081*08  105*10  129*20
010*01  034 02  058*04  082*08  106*10  130*20
011 01  035 02  059*04  083*08  107*10  131*20
012 01  036 02  060 04  084 08  108*10  132*20
013*02  037*00  061 04  085 08  109*10  133*20
014*02  038*00  062*00  086 08  110*10  134 20
015*02  039*04  063*08  087*00  111 10  135 20
016*02  040*04  064*08  088*00  112 10  136 20
017*02  041*04  065*08  089*00  113*20  137*00
018*02  042*04  066*08  090*00  114*20  138*00
019*02  043*04  067*08  091*10  115*20  139*00
020*02  044*04  068*08  092*10  116*20  140*40
021*02  045*04  069*08  093*10  117*20  141*40
022*02  046*04  070*08  094*10  118*20  142*40
023*02  047*04  071*08  095*10  119*20  143*40
    TOTAL * =409    FIRST * =  0    LAST * =514
 C=  0 R=514 (R-C)=+514( 20.56nS) CL=0 LEVEL=0 RDY
```

Figure 10-107. Effect of Specified Sample Rate and Trace Condition.

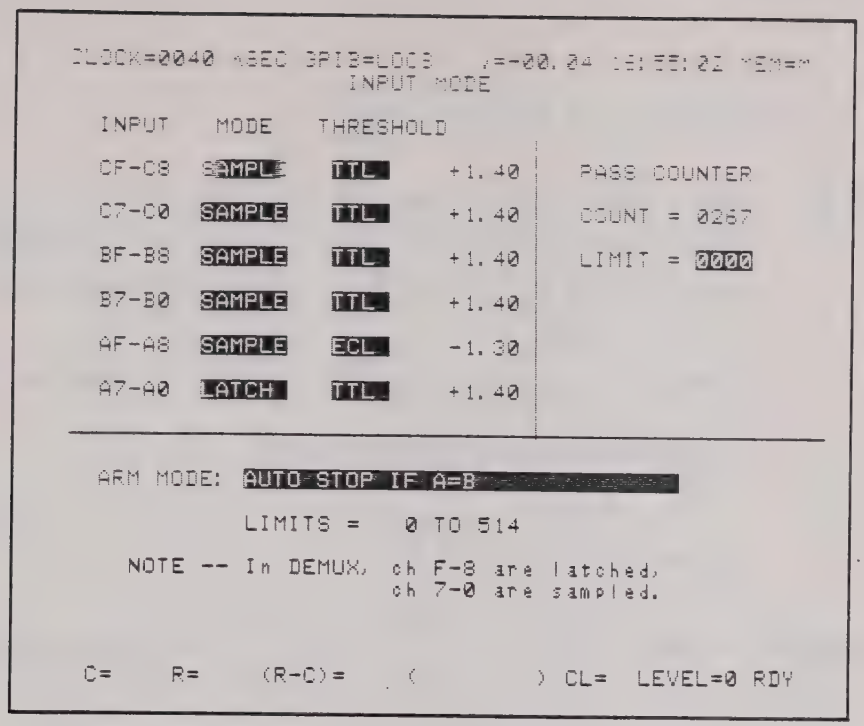


Figure 10-108. 267 Recordings Compared Before Match.

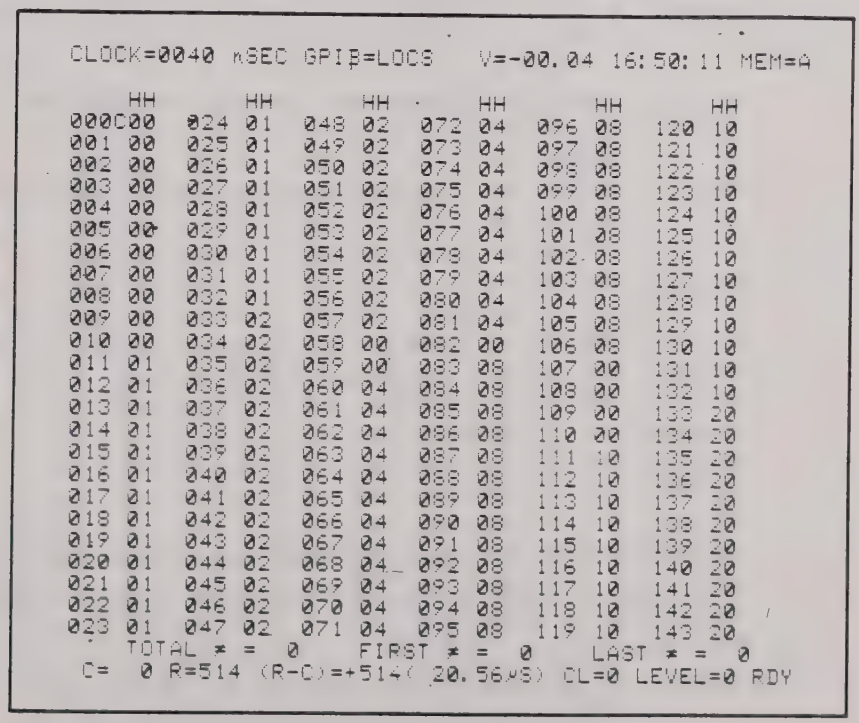


Figure 10-109. Identical Recordings.

10.2.7.6 Auto Stop if A ≠ B Within Limits

SET UP: Once the problem area has been narrowed down, it often isn't necessary to compare the entire recording, only portions of it. To do this, change the arm mode.

Press [INPUT MODE] , [△] , [V24 5 L] , then go back to synchronous clocking.

Press [CLOCK SELECT] , [Hx3 1 H] .

RECORD: Press [ARM] , [A→B] , [ARM] to load memory B and initiate the auto arming.

Press [SHIFT] , [+ ◁ SET] , [V24 5 L] , [Hx1 0 G] , twice to set the cursors to frame the area of comparison.

Press [INPUT MODE] to check the cursors' locations (see Figure 10-110).

Press [DATA] , [B] , [+ ▷] , [EDIT] , [DEMUX F V HEX] , [EDIT] .

Rearming does not stop because the inequality is outside the area defined by the cursors (see Figure 10-111).

Press [EDIT] , [+ ▽ SET] twice, [Hx3 1 H] , [EDIT] .

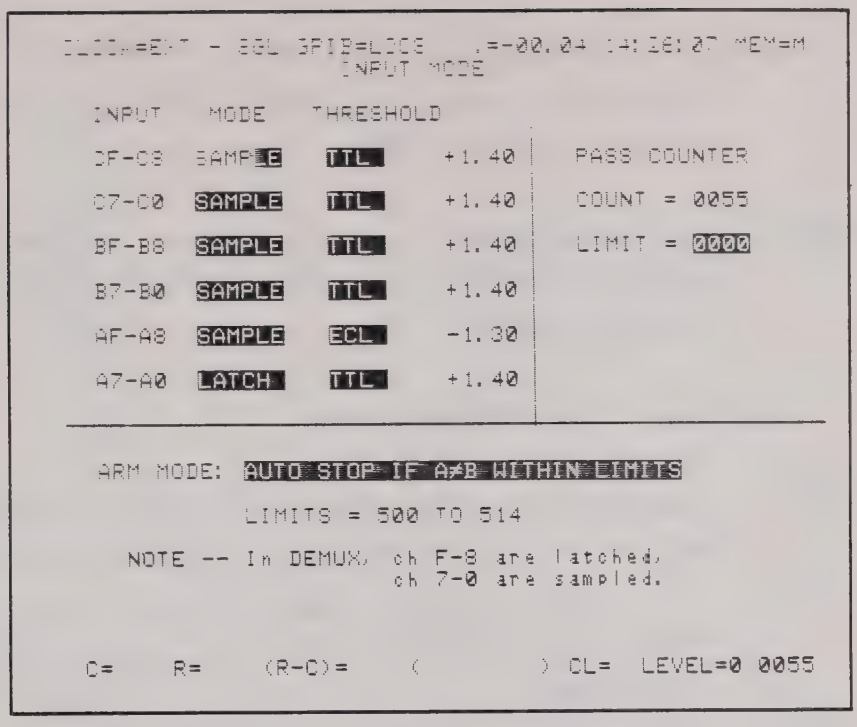


Figure 10-110. Comparison Between Location 500 and 514.

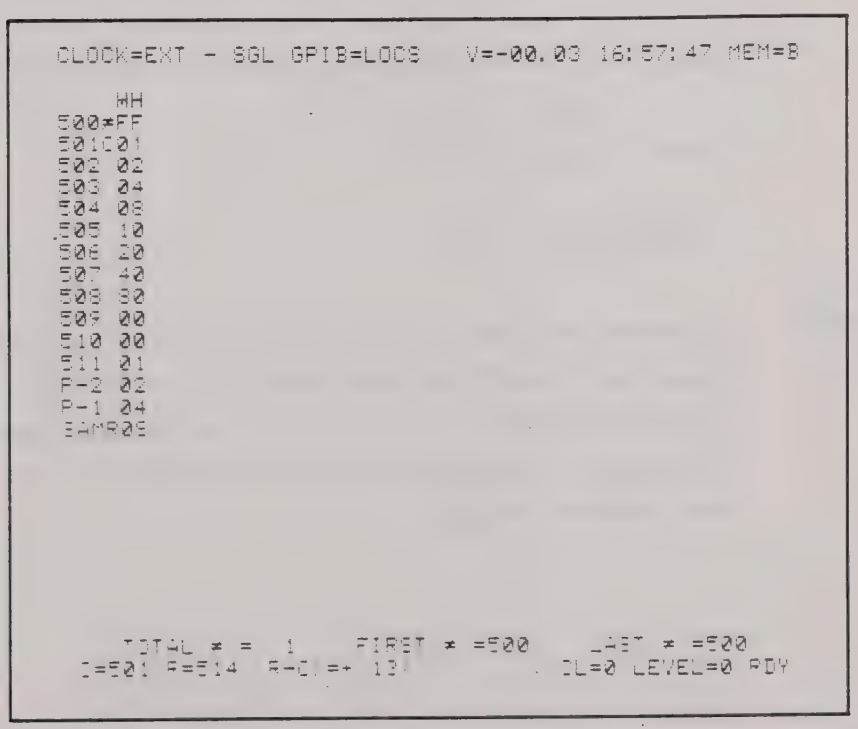


Figure 10-111. Inequality Outside Window.

The auto stop condition is now satisfied as the change is within the cursor limits.

REVIEW: The display should look like Figure 10-112 which shows that an inequality within the limited comparison window stops auto arming.

10.2.7.7 Auto Stop if A = B Within Limits

SET UP: A check for equality similarly may be focused on a smaller area of the recording. Change the arm mode.

Press [INPUT MODE], [△], [PAGE 4 K], [DATA], [B].

RECORD: Press [ARM] to start the recording process.

Since the memories were made unequal in the previous exercise, the rearming could continue indefinitely.

Press [EDIT], [▽ SET], [Hex 0 G], [EDIT].

Recording will stop.

REVIEW: Between the Control Cursor and the Reference Cursor, memories A and B are now identical (see Figure 10-113), which satisfied the auto stop condition. Figure 10-113 shows that arming stops when the samples in the windowed area become the same.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.03  15:35:32 MEM=B

     HH
500≠FF
501C01
502≠12
503 04
504 08
505 10
506 20
507 40
508 80
509 00
510 00
511 01
P-2 02
P-1 04
SAMR08

    TOTAL ≠ =  2     FIRST ≠ =500     LAST ≠ =502
 C=501 R=514 (R-C)=+ 13(          ) CL=0 LEVEL=0 RDY
```

Figure 10-112. Inequality Within Window.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.03  15:35:32 MEM=B

     HH
501C01
502 02
503 04
504 08
505 10
506 20
507 40
508 80
509 00
510 00
511 01
P-2 02
P-1 04
SAMR08

    TOTAL ≠ =  1     FIRST ≠ =502     LAST ≠ =502
 C=501 R=514 (R-C)=+ 13(          ) CL=0 LEVEL=0 RDY
```

Figure 10-113. Samples in Window Same Arming Stops.

10.3 POWER UP TEST

As soon as the power is turned on, the K101-D will beep and start executing an automatic diagnostic routine of six tests. As each test is completed, the next test is automatically run. When all tests are successfully completed, the analyzer beeps again and displays the Clock Select setup screen.

If an error is detected in any of the tests, the name of the failed test is displayed and further testing halted. To run the rest of the power up tests, or to attempt to operate the instrument despite the error, press **NEXT** to continue. When the last test (successful or not) is completed, the Clock Select setup screen is displayed. At this point, since an error has been detected, you should run the appropriate Self-Test diagnostic routine (see paragraph 10.4, Self Test). Table 10-2 lists the power up error messages and the action you should take to respond to these messages. The following paragraphs briefly describe the six power up tests.

10.3.1 K101-D ROM TEST

A total of 16 EPROMs are individually tested against known check sums. The failure display uses an 8 x 2 grid to indicate the physical location of the bad ROM on the K101-D MPU PC board (see Figure 10-114). Any failure can cause incorrect operation of the unit.

10.3.2 K101-D RAM TEST

A total of sixteen 64K RAMs are tested and any failures are displayed in a grid indicating the faulty RAM location on the K101-D MPU PC board (see Figure 10-115). Any failure can cause incorrect operation of the unit.

Table 10-2. Power Up Test Error Messages

Error Message	Appropriate Response
1. ROM: see Figure 10-114	Advise Gould repair facility
2. RAM: see Figure 10-115	Advise Gould repair facility
3. Power supply: see Figure 10-116	Run indicated Self-Test and advise Gould repair
4. CMOS RAM checks in error	See paragraph 10.3.4. Advise Gould repair facility if error does not clear
5. USART: see Figure 10-117	
6. Stuck key	See paragraph 10.3.6. Advise Gould repair facility as to which key is stuck

```
ROM CHECKSUM ERROR:

   MAP OF ROMS ON MPU BOARD (G=GOOD, X=BAD)

   COL→   1   2
   ROW↓
      A   G   G
      B   G   G
      C   G   G
      D   G   G
      E   G   G
      F   G   G
      G   G   G
      H   G   X

PRESS "NEXT" TO CONTINUE
```

Figure 10-114. ROM Test Grid.

```
MPU MEMORY FAILURE:

   MAP OF RAMS ON MPU BOARD (G=GOOD, X=BAD)

   COL→   3   4   5   6
   ROW↓
      A       X       G
      B       G       G
      C       G       G
      D       G       G
      E       G       G
      F       G       G
      G       G       G
      H       G       G

PRESS "NEXT" TO CONTINUE
```

Figure 10-115. RAM Test Grid.

10.3.3 POWER SUPPLY TEST

Each of the power supply's voltage outputs is tested on a pass/fail basis. If any supply is out of tolerance, the testing stops and a message is displayed indicating which power supply failed (see Figure 10-116). Power supply tolerances are discussed in paragraph 10.4. A failure may or may not cause improper operation of the unit, depending on the nature of the failure.

10.3.4 CMOS RAM TEST

The stored data are tested against a check sum also stored in the CMOS RAM. (This is not the same as the CMOS RAM Self-Test.) A failure causes an error message (CMOS RAM CHECKSUM ERROR) to be displayed. An error indicates that the unit will not properly recall the recording setup parameters previously stored, nor correctly save new ones.

The appearance of the error message does not necessarily mean a component has failed. The source could be an intermittent, "soft" error. The following procedure will clear such a soft error:

Press CHOICE NEXT . Wait for Clock Select to be displayed.

Press SHIFT , RECALL , and SAVE .

This loads the default setups from ROM into the CMOS RAM. If the original error was not caused by a component failure, the CMOS RAM CHECKSUM ERROR should not appear on the next power up and the CMOS memory should operate correctly. You can test this by changing any parameter from its default value, pressing **SAVE**, then **RECALL**, and seeing if the changed parameter is still there as it should be.

10.3.5 USART ERRORS

The status of the communication I/O USART is checked for failures. USART failures may cause incorrect operation of the unit. See Figure 10-117 for USART error messages.

10.3.6 KEYBOARD TEST

Each one of the keys on the front panel keyboard is tested for a NOT PRESSED condition. If a pressed key is observed, the unit displays an error message: STUCK KEY. Press one key at a time; keys that are not stuck cause the unit to beep when pressed. Stuck keys must be repaired in order to continue operation of the unit.

10.4 SELF-TEST

Self-Test is selected by pressing **SHIFT**, then **SELF TEST.** The screen will display a menu of the various tests that can be run (see Figure 10-118). To run a specific test, move the cursor up or down (field up or field down) to the desired test then press **NEXT.** Depending on the test, the unit either starts an actual test or displays a more detailed submenu. To run a specific submenu test, again move the cursor to the desired test and press **NEXT.** To exit a submenu and return to the main menu, press **PREV.** To exit Self-Test altogether, press **PREV** while in the main Self-Test menu.

A confidence test generally runs all the specific tests listed beneath it. At the completion of a confidence test, the display says only whether the tests passed or failed; no detailed failure information is given. At the completion of the confidence tests (there is no screen indication showing that a test is being run while it is executing) END OF TEST and test PASSED, or FAILED are displayed. Have patience. Some tests (such as trace control) take several minutes to complete. Also, failures will extend the testing time.

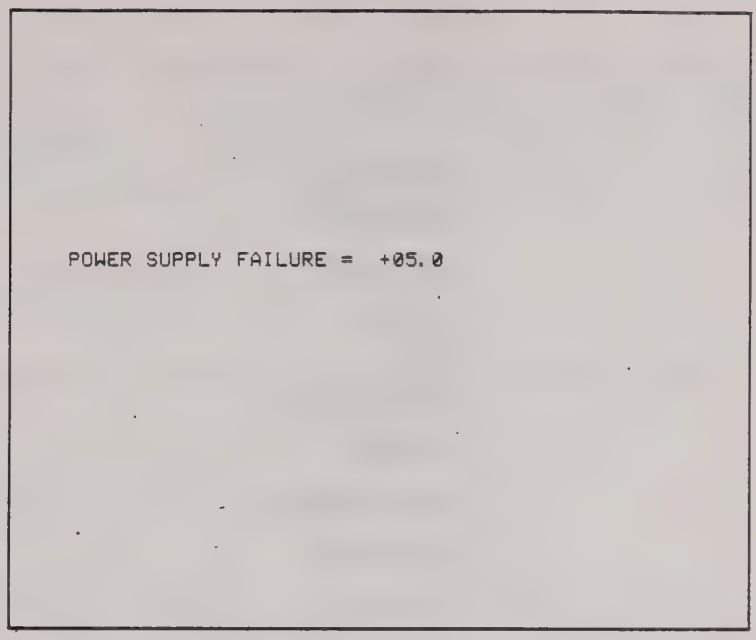


Figure 10-116. Power Supply Error Messages.

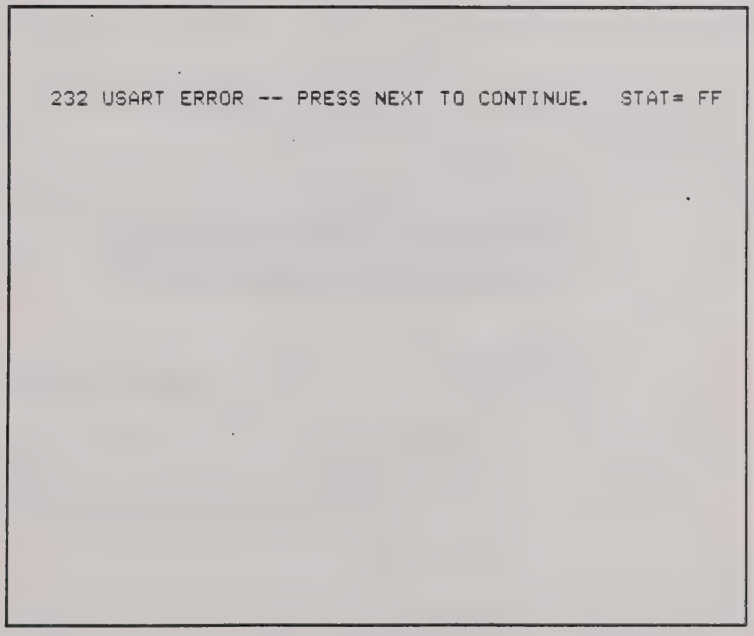


Figure 10-117. USART Error Messages.

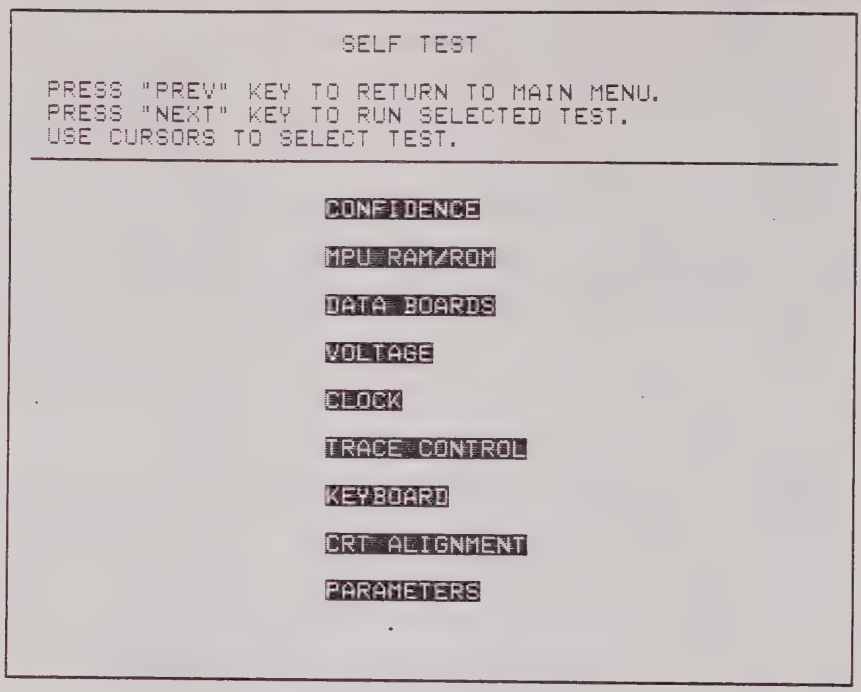


Figure 10-118. Main Menu When First Entering Self-Test.

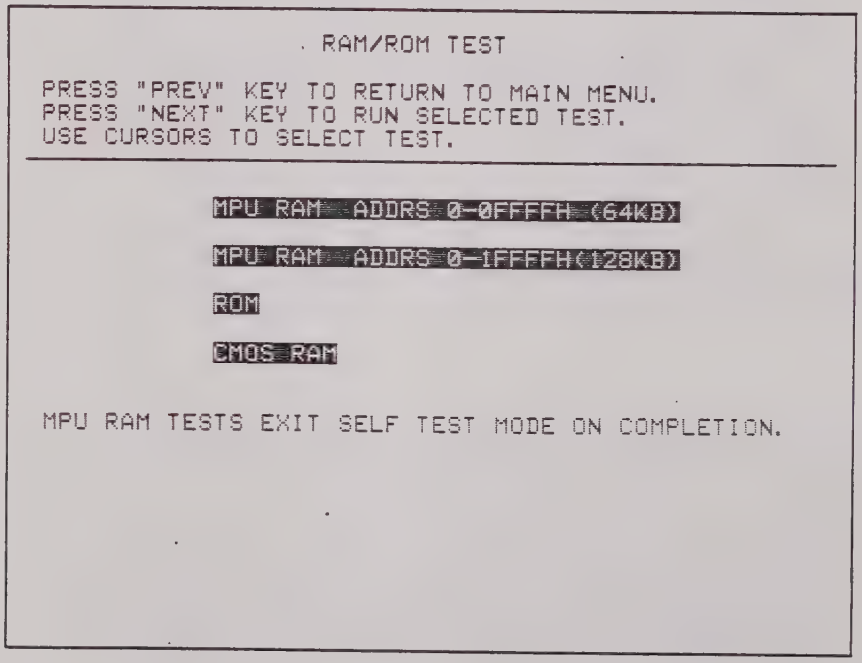


Figure 10-119. MPU RAM/ROM Test Submenu.

Running the specific diagnostic tests individually results in an error summary listing of the type and number of failures as well as specific failure information. The format of this detailed error information is specified in the Parameters screen (discussed later in this section).

10.4.1 CONFIDENCE TEST

Runs all tests in the main menu except for Keyboard, CRT alignment, and Parameters.

10.4.2 K101-D MPU RAM/ROM

When this test is selected, the submenu appears as shown in Figure 10-119.

10.4.2.1 **MPU RAM (64K)**

This test checks the first half of the memory RAM on the MPU board. Failures are displayed on a grid showing faulty RAM locations on the MPU board. This test is also run during power up testing. Failures may or may not affect system operation. Failures can be listed by each bad memory location when using the scroll selection of the Parameter screen. Note that upon completion of this test, Self-Test mode is automatically exited.

10.4.2.2 **MPU RAM (128K)**

This test checks all of memory RAM on the MPU board. It operates identically to the MPU RAM (64K) test.

10.4.2.3 **ROM**

This test verifies the check sum of all 16 EPROMs on the MPU board. Any failures are displayed on a grid, to show the location of the faulty ROM. This test is also run during power up testing.

10.4.2.4 **CMOS RAM**

This test checks the ability of the CMOS RAMs to store new data. Failures are listed as specified by the Parameter screen. A failure indicates the unit will fail the CMOS RAM test (of the power up tests), and that the unit will power up with unwanted recording setups. Refer to paragraph 10.3.4 for instructions to clear CMOS RAM errors.

10.4.3 DATA BOARDS

When this test is selected, the submenu shown in Figure 10-120 is displayed.

10.4.3.1 **Confidence**

This test runs all three data board tests.

10.4.3.2 **Data Board A**

When this test is selected, the submenu shown in Figure 10-121 is displayed.

10.4.3.3 **Confidence Test**

Runs all of the tests on the specific data board.

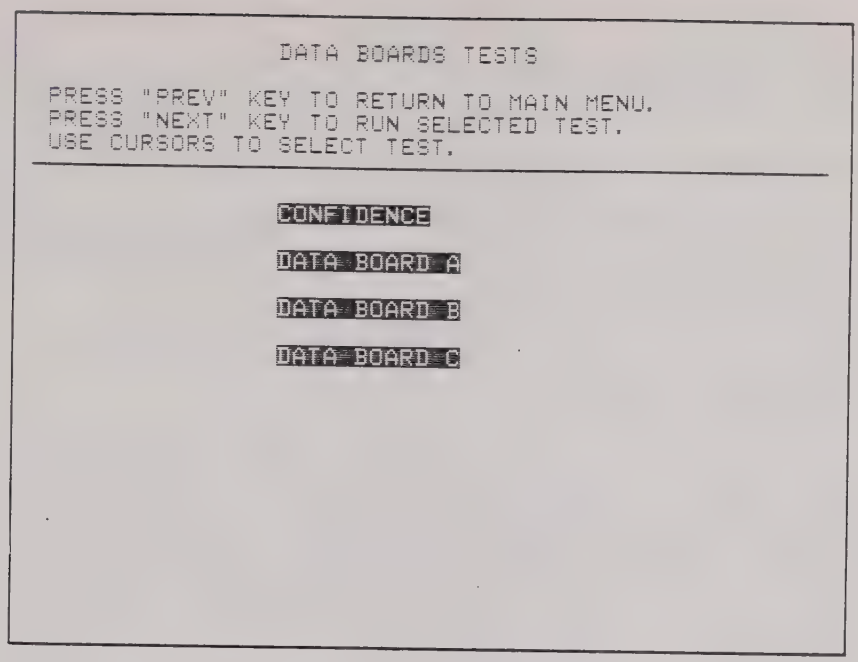
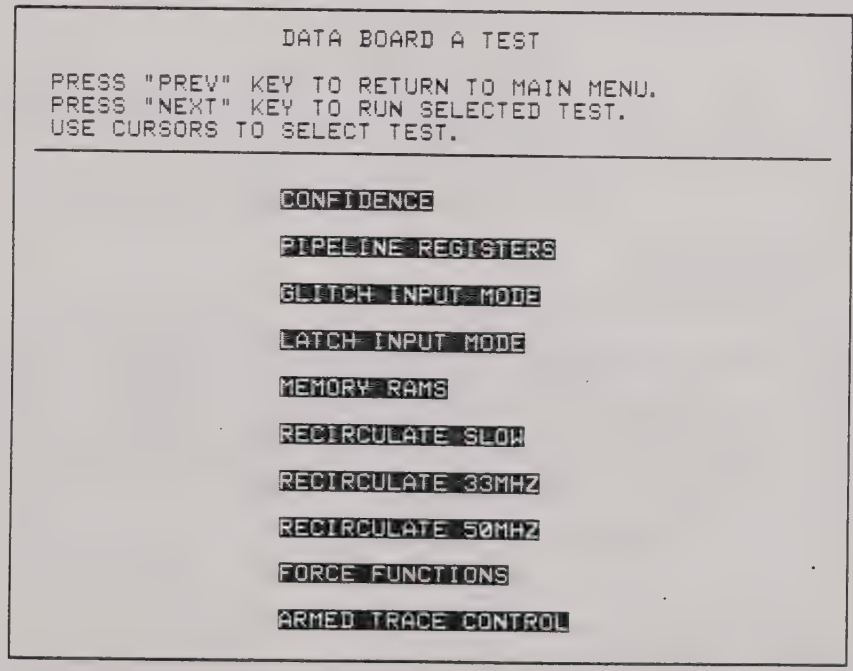


Figure 10-120. Data Board Tests Submenus.



Note: The Menus for boards B and C are identical.

Figure 10-121. Data Board A Submenu.

10.4.3.4 **Pipeline Registers**

This test checks the pipeline register circuitry on the data board. A failure indicates which of that section's 16 inputs will not record properly. Failures are displayed to show the data expected and data actually recorded in hex words.

10.4.3.5 **Glitch Input Mode**

This test checks the ability of all the inputs to detect glitches while in the glitch mode. Failures are displayed to show hex data words that indicate which inputs are not detecting properly. If this is the only test that failed, the only operation that should be affected is that of glitch capture.

10.4.3.6 **Latch Input Mode**

All of the latch inputs are tested for proper operation. For failures, readings similar to those for other data board tests are displayed. Typically, if the unit fails this test, an input is not sampled.

10.4.3.7 **Memory RAMs**

This test checks the ability of the high-speed memory RAMs to store information. Note that if there are failures in the previous data board test, the memory RAMs appear to be bad but may not be. Failures are displayed in hex as in previous tests. Typically, if the memory RAMs fail, recorded information is incorrect.

10.4.3.8 **Recirculate Slow**

This is a slow-speed test of the capability of the data board to feed information out of the memory RAM and then back into RAM. A failure in

this process may not be apparent when making a normal recording unless certain functions are performed with the logic analyzer. Failures are displayed in hex.

10.4.3.9 **Recirculate 33 MHz**

This is the same test as Recirculate Slow, except the test runs at 33 MHz.

10.4.3.10 **Recirculate 50 MHz**

This is the same test as Recirculate Slow, except the test runs at 50 MHz.

10.4.3.11 **Force Functions**

This test checks the recording control of the data board. If failures are observed, more than one channel may be inoperative. (Test mnemonics require a technical description from the factory.)

10.4.3.12 **Armed Trace Control**

This test checks trace control functions within the data board for errors. (Error descriptions require further technical information from the factory.) Failures may or may not cause improper operation of the unit, depending upon the failure and nature of the trace control functions being performed.

10.4.3.13 **Confidence**

This test runs all tests except for DVM and Calibrate. Note that the probes must be connected before running this test.

10.4.3.14 **ADC Calibration**

This test checks the voltage measurement circuits by measuring the +10.00 V reference. An error here may indicate the DVM circuitry is faulty or out of calibration. A DVM fault can cause incorrect failures to be displayed on any voltage test. Another cause could be the +10.00 V reference being out of tolerance. Refer to paragraph 10.4.3.22 for information on the reference supply.

10.4.3.15 **Power Supply Test**

This test checks that each power supply is within set tolerances. Refer to paragraph 10.4.3.21 for power supply tolerances. Each failed power supply is displayed. The tested power supplies are the +15, -15, -10, -5.2, and -2 V battery and the +10 V reference supply.

10.4.3.16 **Threshold Source**

There are four different threshold selections available. The circuitry that generates the four voltages (TTL, ECL, VAR A, VAR B) is tested for accuracy. Any failures displayed indicate that the threshold voltage is not accurate on any probes that are trying to use that threshold.

10.4.3.17 **Threshold Selection**

This test verifies that each probe can be operated on TTL, ECL, VAR A, or VAR B. A failure is displayed if any threshold selector does not put out the correct voltage. This test may fail if there was a failure in the Threshold Source test.

10.4.3.18 **Probe Loading**

This test verifies the accuracy of the load the input probe has on the threshold voltage. If there is no connection to a probe, the voltage measures too high and is indicated as a failure. Also, if the probe is bad, it may short the voltage such that it measures too low, and so indicates a failure. The probes must be connected to run this test.

10.4.3.19 **Variable A/B**

This test checks the linearity of the variable threshold voltages. This test measures linearity at the output going to the input probe. A failure indicates the variable voltages are bad or out of tolerance. Recordings are not affected, unless the threshold that failed is selected. The probes must be connected before running this test.

10.4.3.20 **DVM**

This test requires the installation of DVM cables to the input probe connector. Without jumpers, this test will fail. Install a jumper from the +DVM input to pin 14 of the A8 section input probe connector (lower right hand pin). Install a jumper from the -DVM (ground) to pin 14 of the A0 section input probe connector. The jumpers connect the threshold voltages to the DVM inputs. The external DVM circuitry is tested for accuracy and linearity. If there are threshold failures, the DVM test may fail. Specific voltage measurement failures are displayed.

10.4.3.21 **Calibrate**

This test displays the voltages actually measured and the acceptable tolerances. The display is continually updated every few seconds. Power supply voltages can be adjusted by monitoring this display, but it is recommended that you adjust power supplies by the calibration

procedure. The display that is observed while in the Calibrate mode is shown in Figure 10-122.

The following is a list of the various power supply voltages and the associated circuitry to which they provide power:

a. ±15 V -- Display and threshold circuitry
b. ±10 V -- Threshold voltage generation circuitry
c. -5.2 V -- ECL circuitry within the unit
d. +5 V -- TTL circuitry within the unit
e. -2 V -- Many ECL pull-down resistors
f. Battery -- CMOS RAMs

10.4.4 VOLTAGE TEST

When this test is selected, the submenu shown in Figure 10-123 is displayed.

10.4.5 CLOCK

When this test is selected, the submenu shown in Figure 10-124 is displayed.

10.4.5.1 **Confidence**

This test runs both the Clock Frequency and the Level Memory tests.

10.4.5.2 **Clock Frequency**

This test checks the various internal clock frequencies on which the unit operates. The multiplier frequencies and actual measurements are displayed if a failure is noted.

CALIBRATE

SUPPLY NOMINAL	ACCEPTABLE MINIMUM	ACCEPTABLE MAXIMUM	MEASURED AVERAGE	MEASURED P-P
+15.00 V	+14.40	+15.60	+15.02	+0.03
-15.00 V	-15.60	-14.40	-15.03	+0.05
-10.00 V	-10.10	-9.90	-9.99	+0.00
+5.04 V	+4.84	+5.24	+5.02	+0.01
-5.28 V	-5.48	-5.08	-5.20	+0.09
-2.08 V	-2.16	-2.00	-2.09	+0.04
V BATT	+2.34	+4.00	+3.06	+0.00
GND REF	-0.02	+0.02	-0.00	+0.00
+10V REF	+9.96	+10.04	+10.00	+0.00

USE "PREV" TO RETURN TO MENU

Figure 10-122. Typical Calibrate Display.

VOLTAGE TESTS

PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.

CONFIDENCE

ADC CALIBRATION

POWER SUPPLY

THRESHOLD SOURCE

THRESHOLD SELECTOR

PROBE LOADING

VAR A/B

DVM

CALIBRATE

PROBES MUST BE INSTALLED FOR CONFIDENCE TEST AND
FOR PROBE LOADING AND VAR A/B TESTS.
DVM TEST FIXTURE IS REQUIRED FOR DVM TEST.

Figure 10-123. Voltage Test Submenu.

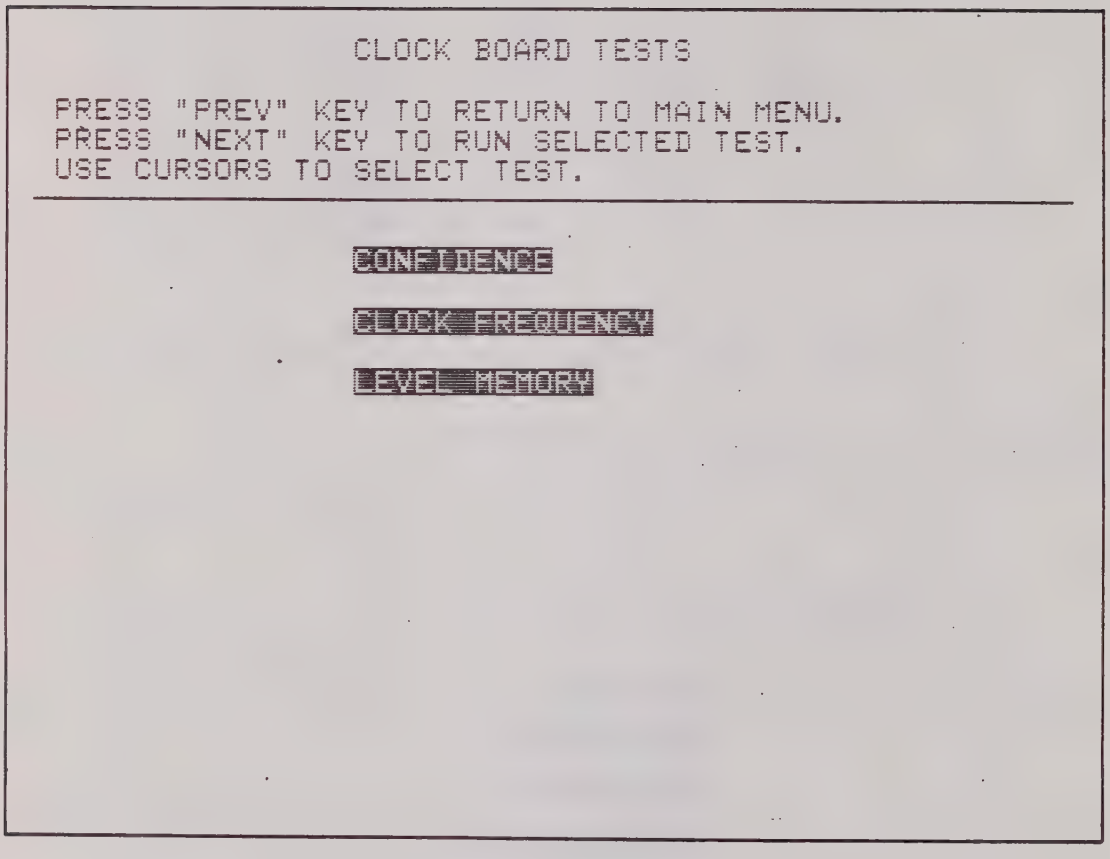


Figure 10-124. Clock Test Submenu.

10.4.5.3 **Level Memory**

This test checks the ability of the level memory RAMs to store the level at which trace control samples were recorded. Failures are displayed by memory location. A failure here indicates the memory will not be accurate.

10.4.6 TRACE CONTROL

When this test is selected, the submenu shown in Figure 10-125 is displayed.

10.4.6.1 **Trace Confidence**

This test runs all of the tests in the menu.

10.4.6.2 **Force Conditions**

This test checks the ability of the unit to perform basic trace control functions. A failure indicates the unit may not perform trace control functions, depending upon the failure.

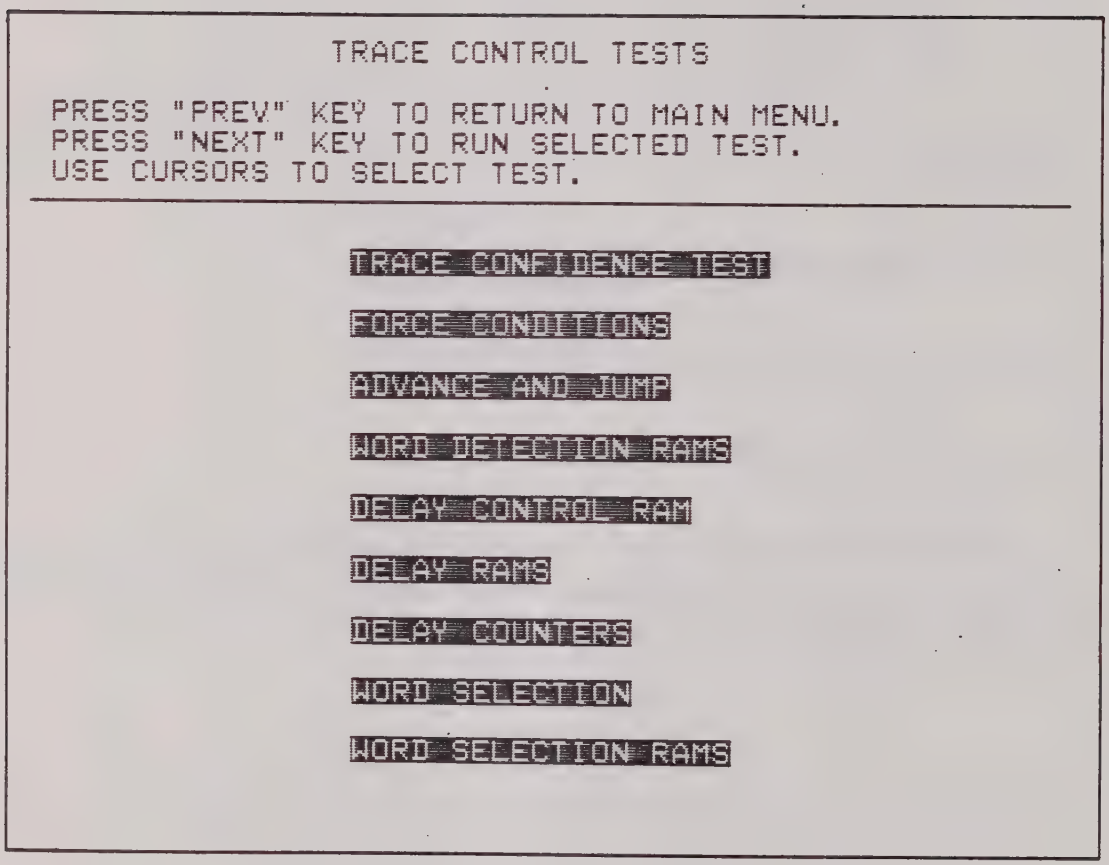


Figure 10-125. Trace Control Test Submenu.

10.4.6.3 **Advance and Jump**

This test checks the ability of the unit to ADVANCE and JUMP to the various levels of trace control. A failure indicates the unit may not record properly, depending upon the failure and the functions the logic analyzer is trying to perform.

10.4.6.4 **Word Detection RAMs**

This test checks the RAMs' capability to store data that control the word detection circuitry. A failure indicates the unit may not recognize the S, J, A, and T word recognizers used in the trace control commands. This test takes several minutes to run.

10.4.6.5 **Delay Control RAM**

This test checks the RAMs' capability to store data that control the delay control circuitry. A failure indicates the unit will not perform delay functions, depending on the failure.

10.4.6.6 **Delay RAMs**

This test checks the ability of the RAMs to store data that control the amount of delay in tracing functions. A failure indicates the unit may not delay by the proper amount of clocks or events, depending on the failure.

10.4.6.7 **Delay Counters**

This test checks the ability of the unit to count the correct number of clocks or events. A failure indicates the unit may not delay by the proper amount when tracing, depending upon the failure.

10.4.6.8 **Word Selection**

This test checks the ability of the unit to recognize each S, J, A, and T word. A failure indicates the word selection circuitry may not tell the word detection RAMs when a condition is satisfied.

10.4.6.9 **Word Selection RAMs**

This test checks the ability of the RAMs to store data that control the word selection circuitry. A failure indicates the unit may not recognize S, J, A, and T words in the trace control commands.

10.4.7 KEYBOARD

When this test is selected, the keyboard test routine is automatically entered and a display appears as in Figure 10-126. The unit is prompting you to press **DATA**. After you press **DATA**, the display changes and prompts you to press **GRAPH**. To complete the test (and exit the test routine) you must press each key in the proper sequence as prompted by the display (by columms, left to right, going up from bottom row to top row). A BAD KEY error message appears if a key is pressed out of sequence or if the key immediately preceeding the one just pressed is actually bad. (In other words, an actual bad key is not indicated until the next key is pressed.) All 56 keys must be pressed before you can exit the test: there is no way to abort the test.

10.4.8 CRT ALIGNMENT

CRT alignment simply provides a test grid on the CRT in order to adjust it for proper visual linearity (see Figure 10-127).

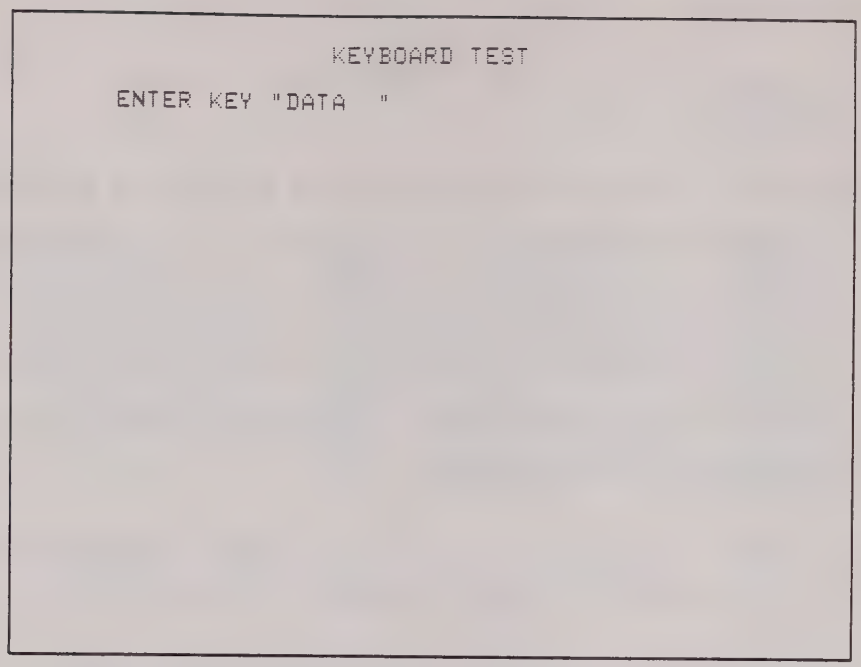


Figure 10-126. First Keyboard Test Display.

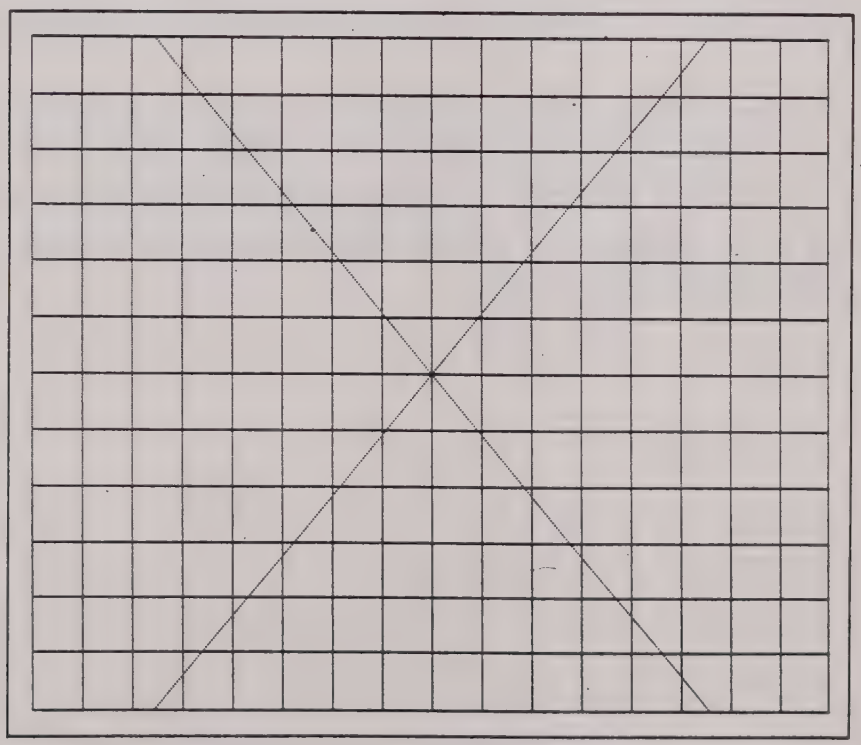


Figure 10-127. Alignment Test Grid.

10.4.9 PARAMETERS

The submenu that is shown when parameters is selected is shown in Figure 10-128. Parameters enhances all of the Self-Test diagnostics. The lower section of the display provides a cumulative total of errors detected during the Self-Test diagnostics. (The totals are reset to zero upon entering Self-Test.) The first field allows you to choose three types of error display modes, which are selectable by the **NEXT** key. The selections are as follows:

a. **Page.** If a failure occurs in a chosen diagnostic test, the unit displays one page (display) of errors only.

b. **Scroll.** If a failure occurs, the display scrolls through the entire list of errors.

c. **No Print.** No errors are displayed even if a failure occurs.

LOOP ON TEST may be selected as YES or NO. If YES is selected the unit continuously performs one Self-Test after another. Once it is looping, the only way to exit Self-Test is to turn off the unit. This allows the instrument to be checked for correct performance over extended use. NO stops after one Self-Test cycle.

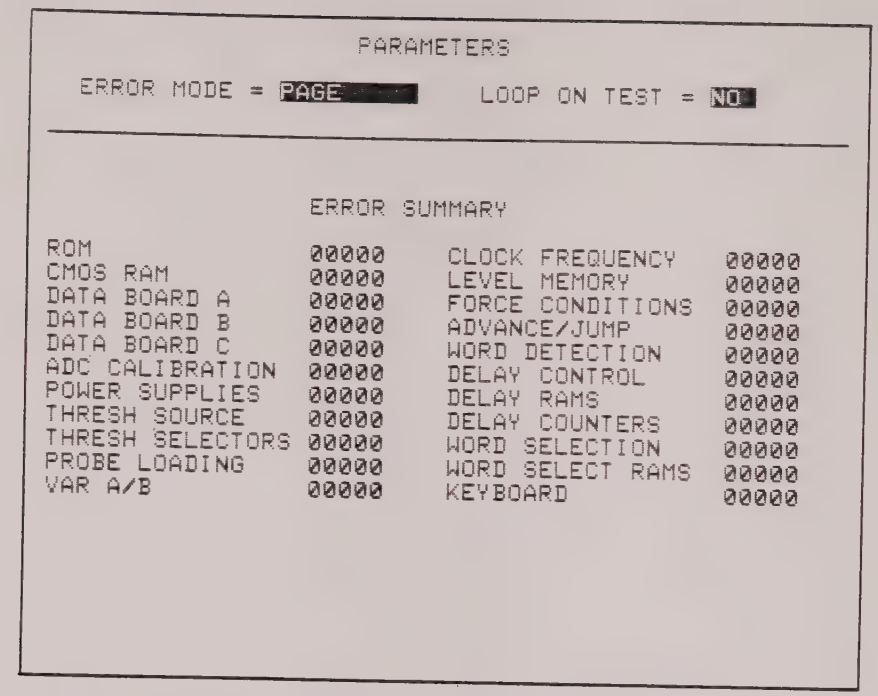


Figure 10-128. Parameters Display Screen.

K101 and K102 Calibration Procedure

Rev. A1
6/16/82

Recommended Test Equipment

Item	MFG	Model No.
3 1/2 Digit DMM	Tektronix	DM501
Oscilloscope	Tektronix	485 or 475A
Frequency Counter	Hewlett-Packard	5316A
0-25 V Power Supply	Hewlett-Packard	6215A
K-101 DVM Leads	Biomation	0114-0057
K-101 Probe Set	Biomation	0114-0254
K-101 Extender Card	Biomation	0950-0135
20 pin .3" IC Clip	Any	Standard
3 mini-clips	Any	Standard
4.7k ohm 1/4w,5%resistor	Any	Standard

I. Display Calibration

To check the unit for proper raster scan display alignment, power-up the unit, depress the "shift" key, then the "selftest" key and move the cursor up 2 times. Then depress the "Next" key. The unit should now be in the CRT alignment mode. The adjustments below are available on the Data Display Board, refer to Figure IA for location of adjustments.

1. Adjust R20 for height
2. Adjust R21 for vertical hold
3. Adjust L1 for width
4. Adjust L2 for horizontal linearity
5. Adjust R29 for focus
6. Adjust R32 for brightness
7. Adjust R47 for vertical linearity

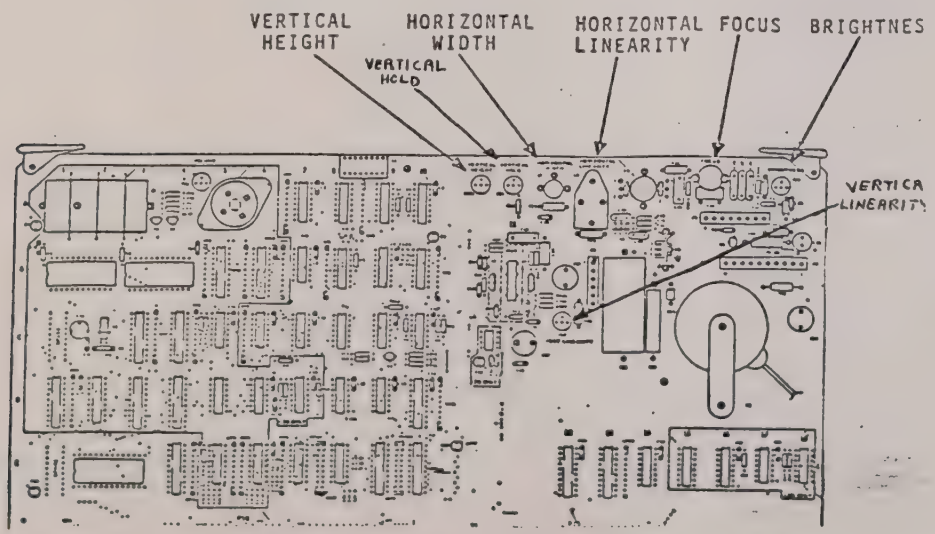


Figure 1A

NOTE: The unit must be allowed to warm up for at least 10 minutes prior to calibration.

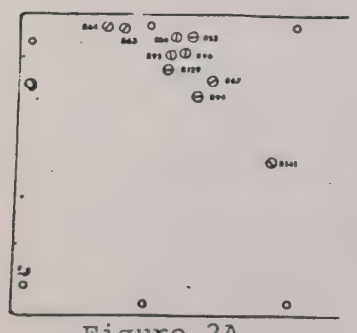
II Power Supply Voltage Adjustment

All input probes should be installed in the unit prior to adjustment. The soft start power supply has each pots purpose labeled. For pot replacement on the old style power supply refer to figure 2A. For measurement test points refer to figure 2B.

1. Remove the bottom cover from the unit and stand the unit on its rear feet.
2. Measure and adjust the -5.2 v. supply to -5.290 volts ± 5 mv.
3. Measure and adjust the +5.0 v. supply to +5.060 volts ± 5 mv.
4. Measure and adjust the -15.0 v. supply to -15.010 volts ± 5 mv.
5. Measure and adjust the +15.0 v. supply to +15.010 volts ± 5 mv.
6. Measure and adjust the -2.0 v. supply to -2.090 volts ± 5 mv.
7. Recheck all voltage measurements. Note that the -5.2 v. supply is the reference for all of the other supplys.

Test Points

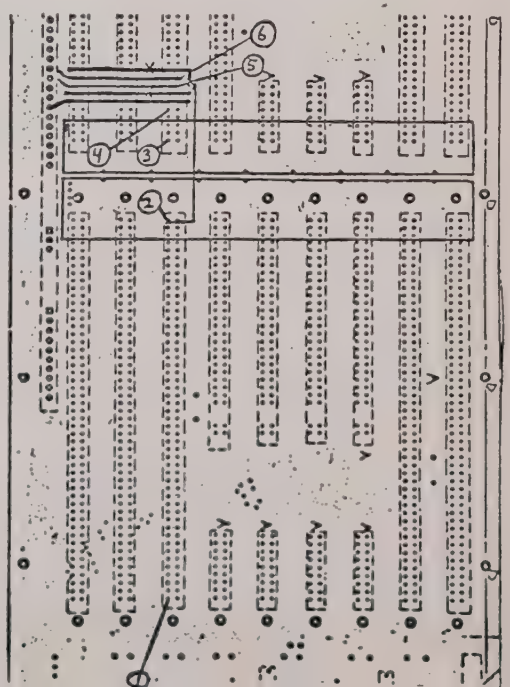
1. +5 v.
2. Gnd
3. -5.2 v.
4. -2.0 v.
5. +15 v.
6. - 15 v.



R64 (-15 V ADJUST)
R63 (+15 V ADJUST)
R54 (+15 V OVERCURRENT)
R53 (-15 V OVERCURRENT)
R95 (-5.2V OVERCURRENT)
R96 (-2 V OVERCURRENT)
R129(-2 V ADJUST)
R87 (-5.2V ADJUST)
R94 (+5 V OVERCURRENT)
R141(+5 V ADJUST)

Figure 2A

Figure 2B. Front of unit



III Power Supply Current Limit Adjustment

The current limits have been set at the factory and should not require calibration. Prior to adjusting the current limits, the voltage settings in Step 2 should be checked and adjusted if necessary. Refer to Figure 2A for pot placement on the Old Style power supply or labeling on the supply for the soft start type power supply. Note that the +15 and -15 volt supplys may not draw enough current to allow the supply to go into current limit. Do not adjust the current limit on the ± 15.

1. Install a complete set of input probes into the unit.

2. Turn on the unit. Adjust the -5.2 v. supply's current limit down (counterclockwise) slowly until the supply shuts down (current limit).

3. Adjust the -5.2 v. supply's current limit pot up approximately 1/2 turn (clockwise).

4. Turn the unit off then back on. Verify the power supply does not go into current limit.

5. Repeat steps 2 through 4 for the +5 volt power supply.

6. Repeat steps 2 through 4 for the -2.0 volt power supply.

7. Recheck all voltage settings. Refer to Section 2.

IV Threshold Voltage Adjustments.

Remove all input probes from the unit. This procedure utilizes a 4.7 k ohm resistor as a load for adjustment of the thresholds. Install a 4.7k ohm resistor between pins 2 and 14 of the AO section input probe connector on the front panel. All voltages will be measured across the resistor. For adjustment, install the resistor in the AO probe connector, refer to Figure 4A for threshold adjustment pot placement.

1. Turn on the unit. Depress the "shift" then "recall" keys. This will put the unit into a default condition for basic recording.

2. Depress the "input mode" key.

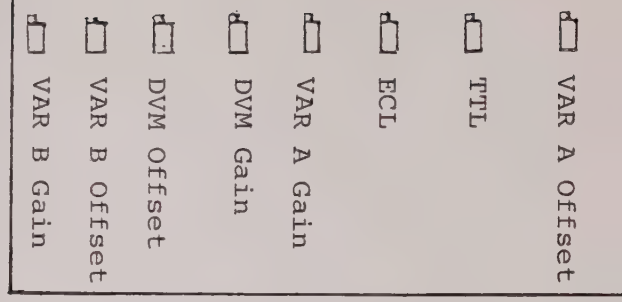
3. Move the cursor up once and hit the "next" key unitl the arm mode reads "auto".

4. Depress the " arm " key. The unit should now be continually taking new recordings, and will automatically update the threshold voltages to the new settings.

5. Change the threshold selection for all probes to "VAR A".

Front of Unit

Figure 4A



6. Set the Var A voltage to 9.98 volts plus or minus.

7. Change the polarity from plus to minus while measuring across the resistor. The voltage should measure 9.98 volts ±25 mv., in both polarity's. Set the voltage to 0.00 volts. It should measure 0.000 volts ±5 mv. Adjust the Var A gain and offset accordingly to meet spec.

8. Repeat steps 5 through 7 for " Var B".

9. Set the threshold selection on all probes to TTL and adjust the voltage to -1.400 volts ± 3 millivolts.

10. Set the threshold selection on all probes to ECL and adjust the voltage to +1.300 volts ± 3 millivolts.

11. Moving the lead resistor to each probe connector, measure the voltages for the correct spec. as in steps 6 through 10.

V. DVM Circuit Calibration

1. Turn on the unit, it should come up in the clock select mode.

2. Input +20.00 volts D.C. ± 5 mv into the DVM inputs on the front panel, noting the voltage reading at the top of the display.

3. Reverse the polarity of the input voltage. Note the reading at the top of the display. Adjust the DVM gain and offset accordingly until the DVM reads 20.00 volts ± .01 in both polarity's and 0.00 with no voltage input.

4. Depress the "shift" then "selftest" keys. Move the cursor down to the voltage test and depress the "next" key. Move the cursor up once and depress the "next" key. The unit should now be in the voltage calibrate mode.

5. Observe all of the voltages in the calibrate mode. Although the voltage tolerances indicated in the calibrate mode are wider, it is necessary that the readings are within the following ranges: (see top of next page)

Voltage	Minimum Acceptable	Maximum Acceptable
+15	+14.90	+15.10
-15	-15.10	-14.90
-10.00 reference	-10.04	- 9.96
+5	+ 5.02	+ 5.08
-5.2	- 5.31	- 5.25
-2.	- 2.12	- 2.07
+10.00 reference	+ 9.97	+10.03

6. DVM test. This test requires DVM cables to be connected. The DVM "input" on the front panel must be connected to the A8-F section input probe connector pin number 14. The DVM "GND" on the front panel must be connected to the A0-7 section input probe connector pin number 14.

   Move the cursor to the DVM test and depress the "next" key. The display should say "end of test"; listing no errors.

7. Run all of the voltage self tests without input probes installed, and all tests should pass except the probe loading test. Install all of the input probes and run the voltage self tests. All of the tests should pass.

VI. High Speed Clock Calibration

1. Turn power off, remove the clock board, and place on an extender. Turn power back on.

2. Refer to figure 6A (Clock Board) for location of parts and test points.

3. Connect the frequency counter to IC 12C, Pin 12, using pin 6 of the same device for ground.

4. Adjust variable capacitor C8 to obtain a frequency reading of 100 mhz $\pm$ 0.1 mhz.

5. Disconnect the frequency counter, and replace it with an oscilloscope probe, using the same signal and ground pins. Use the shortest possible ground lead on the probe.

6. Adjust R19 until the 100 mhz clock waveform is as symmetrical as possible, and centered on an ECL threshold of -1.3 v.

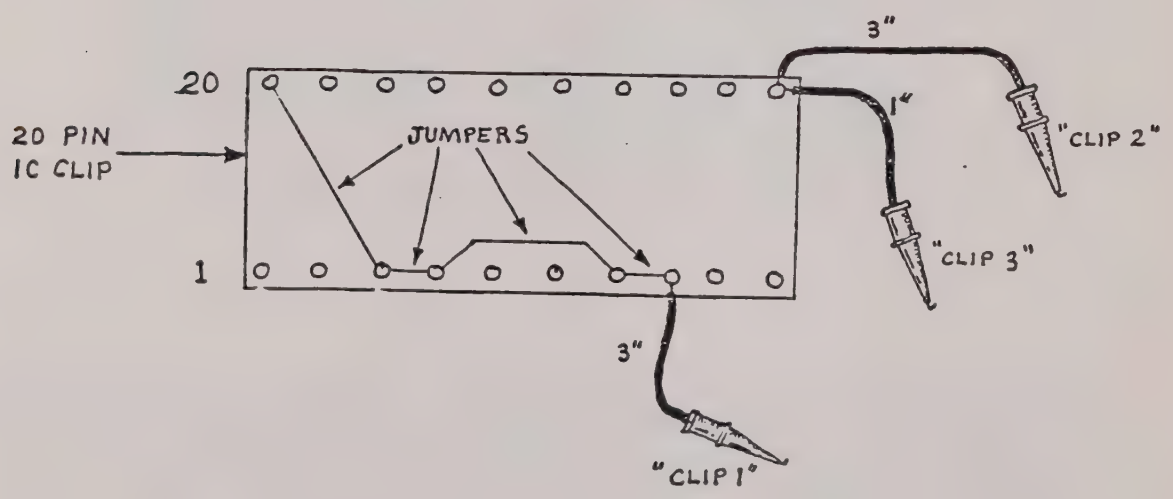
VII Real-Time Clock Calibration

1. Refer to figure 7A of the display board for part locations and test points.

2. Turn power off, place data display board on an extender, and apply power to the unit.

   Note: It is not necessary to re-connect the video cables, only the flyback high-voltage lead!

3. Using the IC clip and the mini clips, construct a test jig according to the drawing below



4. Carefully place the clip on IC, 4D-being sure to watch for proper orientation.

5. Connect "clipl" to IC 3D pin 8, connect "clip 2" to IC 3D pin 11, and "clip 3" to pin 10 of the IC clip.

6. The clock is now in the test mode.

7. Connect the frequency counter to IC 2D pin 9, and place the counter in the "period" mode.

8. Adjust variable capacitor C10 for a period reading of 976.5625 us, ±.0019 us.
9. This allows an initial accuracy of approximately ±5 seconds per month.

Figure 6A

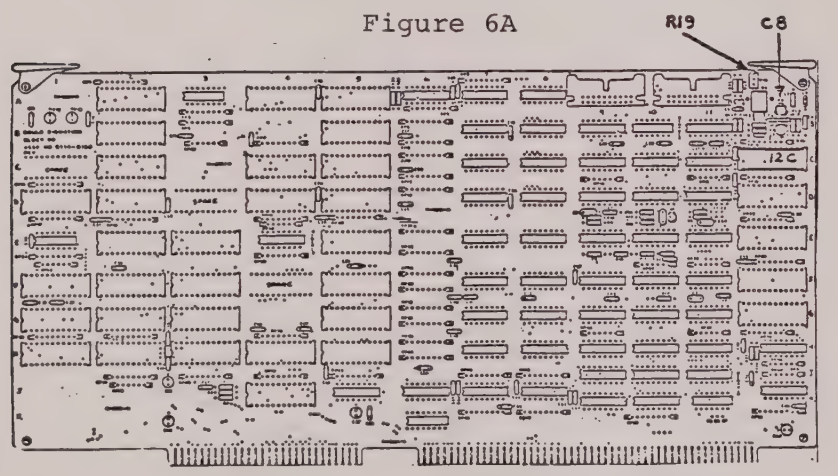
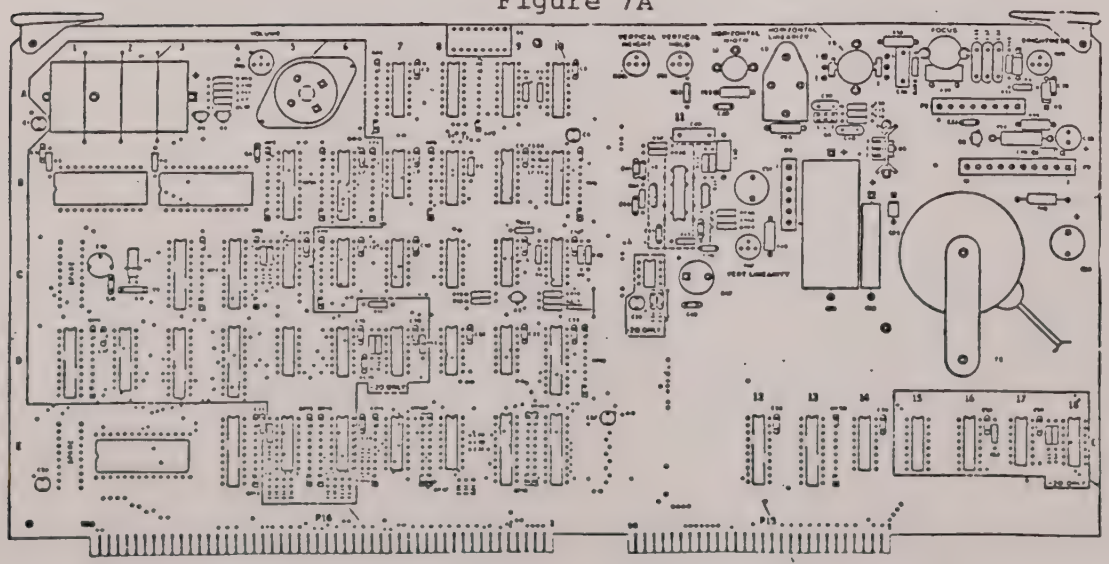
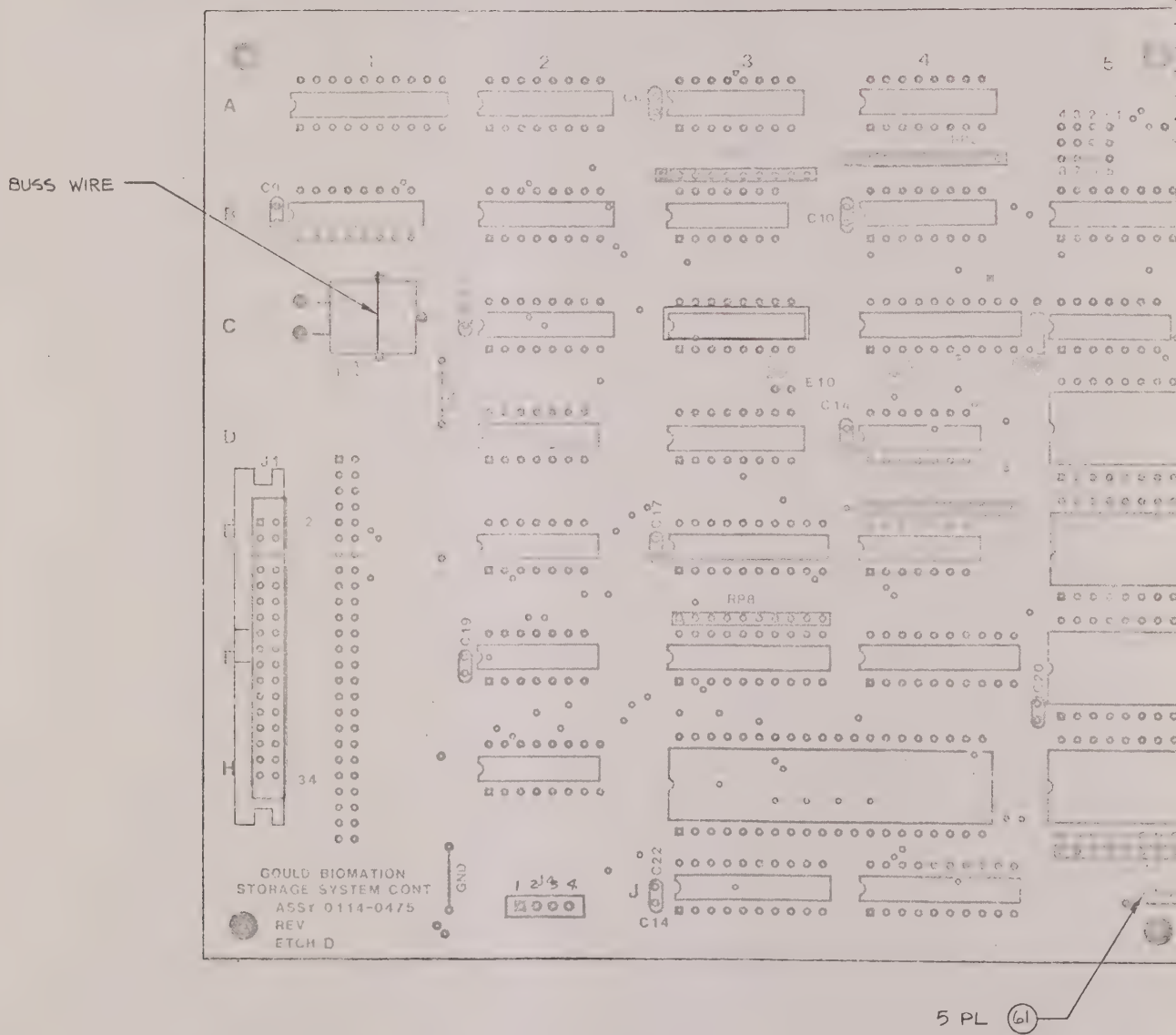


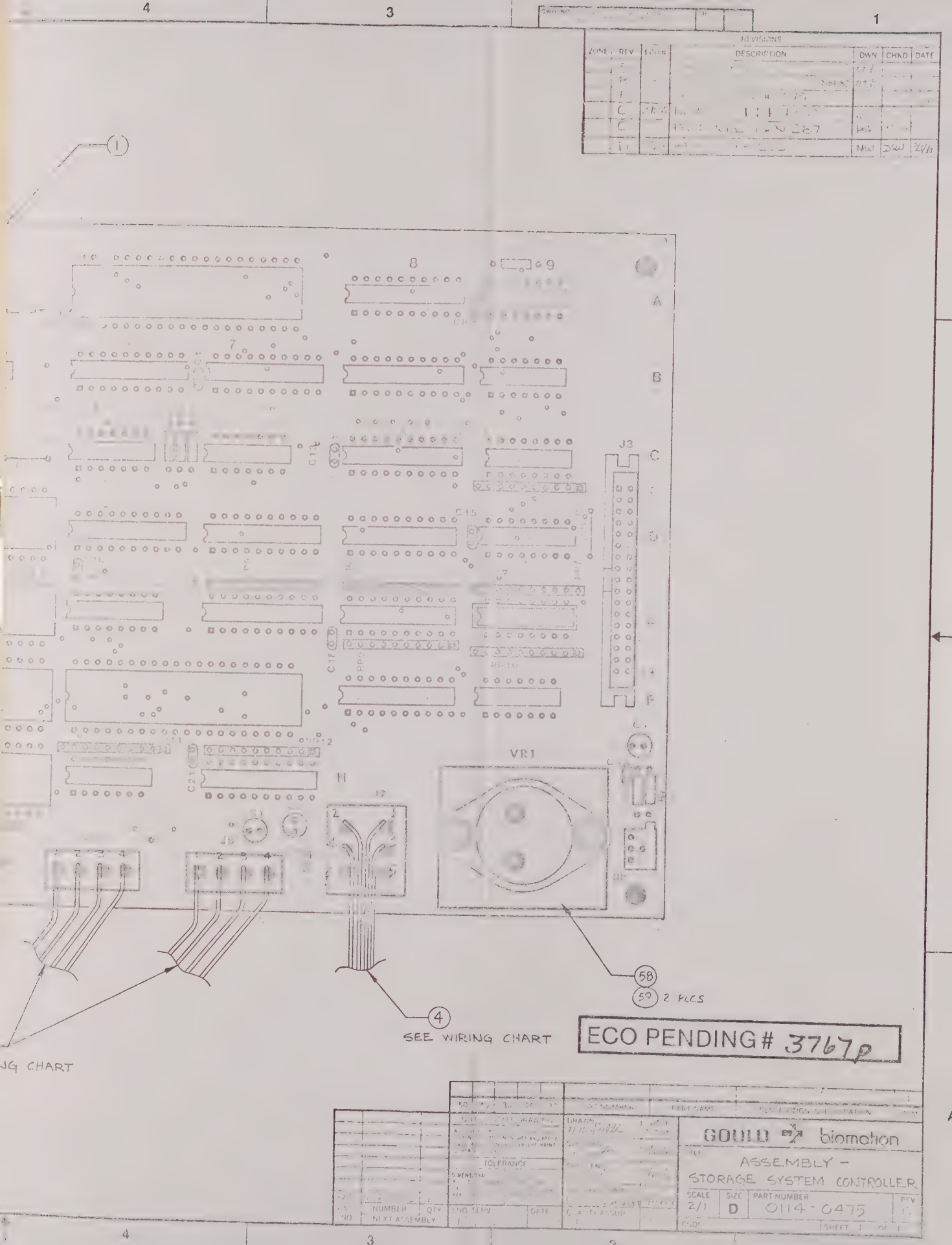
Figure 7A





WIRING CHART	
CONN + PIN	COLOR
J5, J6, J7 - 1	WHT
J5, J6, J7 - 2	BLK
J5, J6, J7 - 3	BLK
J5, J6, J7 - 4	BLK

(5)
SEE WIR



REVISIONS
ZONE
REV
DESCRIPTION
DWN
CHKD
DATE
1
8
9
A
7
B
J3
C
C15
D
F
VR1
H
J7
J6
2 3 4
58
59
2 PLCS
4
SEE WIRING CHART
NG CHART
ECO PENDING # 3767p
GOULD biomation
ASSEMBLY -
STORAGE SYSTEM CONTROLLER
SCALE
2/1
SIZE
D
PART NUMBER
0114-0475
REV
SHEET
NUMBER
QTY
NEXT ASSEMBLY
TOLERANCE
ENG SERV
DATE

ITEM	QUANTITY PER ASSEMBLY									PART NUMBER	PART NAME
	-50	-60	-70	-80	-50	-40	-30	-25	-10		
1									1	0114-0477	PWB
2									1	0114-0476	P.C. [illegible]
3									1	0114-0479	I.C. PWB
4									1	0114-0429	Cable Assy
5									2	0114-0481	Cable Assy
6									1	1700-0102	I.C. LM350
7									2	1800-0085	I.C. 7407
8									1	-0097	I.C. 7406
9											
10									1	-0106	I.C. 74LS02
11									1	-0109	I.C. 74LS08
12									1	-0110	I.C. 74LS10
13									5	-0115	I.C. 74LS74
14									5	-0125	I.C. 74LS161
15									1	-0181	I.C. 74LS151
16									3	-0191	I.C. 74LS138
17									1	-0216	I.C. 74LS32
18									2	-0217	I.C. 74LS153
19									4	-0231	I.C. 74LS273
20									1	-0237	I.C. 74LS139
21									3	-0240	I.C. 74LS244
22									3	-0267	I.C. 74LS240
23									3	-0268	I.C. 74LS245
24									1	-0293	I.C. 74LS374
25									1	-0298	I.C. 74LS373
26									1	-0311	I.C 7438
27									1	1800-0312	I.C 1863

REV	DESCRIPTION	DATE	DWN	CKD
P	REVISED	7/6/82	TMH	

DASH NO.	NUMBER / NEXT ASSEMBLY	QTY
10	[illegible]	1

DWN [illegible]

CHK [illegible]

ENGR [illegible]

MFG. [illegible]

Q.A. [illegible]

[illegible] DESCRIPTION	REFERENCE DESIGNATION	L/M
[illegible]	3C	
[illegible]	9E	
[illegible]ER IN	J7	
[illegible] to Floppy	J5, J6	
[illegible] 3 AMP	VR1	
[illegible] O.C. BUFFER	2E, 2F	
[illegible] O.C. INVERTER	2D	
[illegible] 2-IN NOR	5C	
[illegible] 2-IN AND	7C	
TRIPLE 3-IN NAND	9F	
[illegible] D FLIP-FLOP	6C, 9A, 4E, 4D, 3B	
[illegible]T COUNTER	4A, 4B, 5B, 3A, 2C	
[illegible]-IN MUX	3D	
[illegible] 8 DECODER	6E, 9C, 9D	
[illegible]UAD 2-IN OR	6H	
	2A, 2B	
[illegible]CTAL REGISTER	8D, 8C, 3E, 4C	
DUAL 1 OF 4 DECODER	2H	
[illegible] BUFFER	6D, 8A, 8B	
[illegible] INVERTER	7B, 3F, 4F	
[illegible] BI-DIR BUFFER	8F, 8E, 7D	
OCTAL REGISTER	7H	
OCTAL LATCH	7E	
QUAD O.C. NAND	9B	
[illegible]	6A	

ECO PENDING # 3767

	DATE
	[illegible]
	11-12-8[illegible]
	11-12-8[illegible]
[illegible]	[illegible]
[illegible]	[illegible]

LIST OF MATERIAL

PWB ASSEMBLY

STORAGE SYSTEM CONTROLLER

GOULD biomation

B	0114-C475	REV D
MODEL	SHEET 1 OF 3	

	QUANTITY PER ASSEMBLY									PART NUMBER	PART NA
	-50	-60	-70	-80	-90	-40	-30	-20	-10		
[illegible]									1	1800 - 0342	I.C. [illegible]
[illegible]									[illegible]	[illegible]	[illegible]
[illegible]									1	1800 - [illegible]	I.C. [illegible]
[illegible]											
[illegible]											
[illegible]											
34									4	1820 - 0080	I.C. 6116
[illegible]											
[illegible]									1	3000 - 1500	RESISTOR.
37									1	3000 - 1001	RESISTOR
[illegible]									5	3000 - 2201	RESISTOR
[illegible]									1	3000 - 6806	RESISTOR
40									1	3300 - 0092	POT. , 1
41									8	3700 - 0049	R. PACK
42									4	3700 - 0083	R. PACK
[illegible]									1	3700 - 0100	R. PACK
[illegible]											
[illegible]									18	4010 - 0103	CAP .0
[illegible]									1	4400 - 0043	CAP 47
47									2	4400 - 0045	CAP 33
48											
49									1	5100 - 0021	CRYSTAL
50									1	6000 - 0385 - 04	HEADER ,
51											
52									2	6000 - 0574	CONNECTOR
53											
54									4	6100 - 0122	SOCKET ,
55									3	6100 - 0123	SOCKET
56									[illegible]	6100 - 0120	SOCKET ,
57											

NOTES

DESCRIPTION	REFERENCE DESIGNATION	L/M
[illegible]	2H	
[illegible]	1E	
[illegible]	1E	
2Kx8 RAM	5D, 5E, 5F, 5H	
2, 1/4W, 5%	R1	
1K, 1/4W, 5%	R7	
[illegible], 1/4W, 5%	R2-5,9	
[illegible], 1/4W, 5%	R6	
12 T	R8	
2K, 10PIN, 8 RES.	RP3,5,6,9-13	
K, 10PIN, 9 RES	RP1,2,4,7	
[illegible], 10PIN, 9 RES	RP8	
.50V, 10%	C4-22	
[illegible]V	C1	
[illegible]25V	C2,3	
[illegible] MHz	Y1	
[illegible], KEYBOARD IN	J4	
[illegible] PIN HEADER	J1, J3	
[illegible]	X5D, X5E, X5F, X5H	
[illegible]	6A, 6F, 3H	
[illegible] DIP, LP	3C, 9E	

LIST OF MATERIAL

GOULD biomation

B	0114-0475	REV L

MODEL

SHEET 2 OF 2

ITEM	-30	+30	+70	+80	-50	-40	-30	-20	-10		
50									1	7000-0440-20	HEATSINK
51									2	7011-0002-00	KEPNUT
50											
1									5	9000-0054	WIRE, F

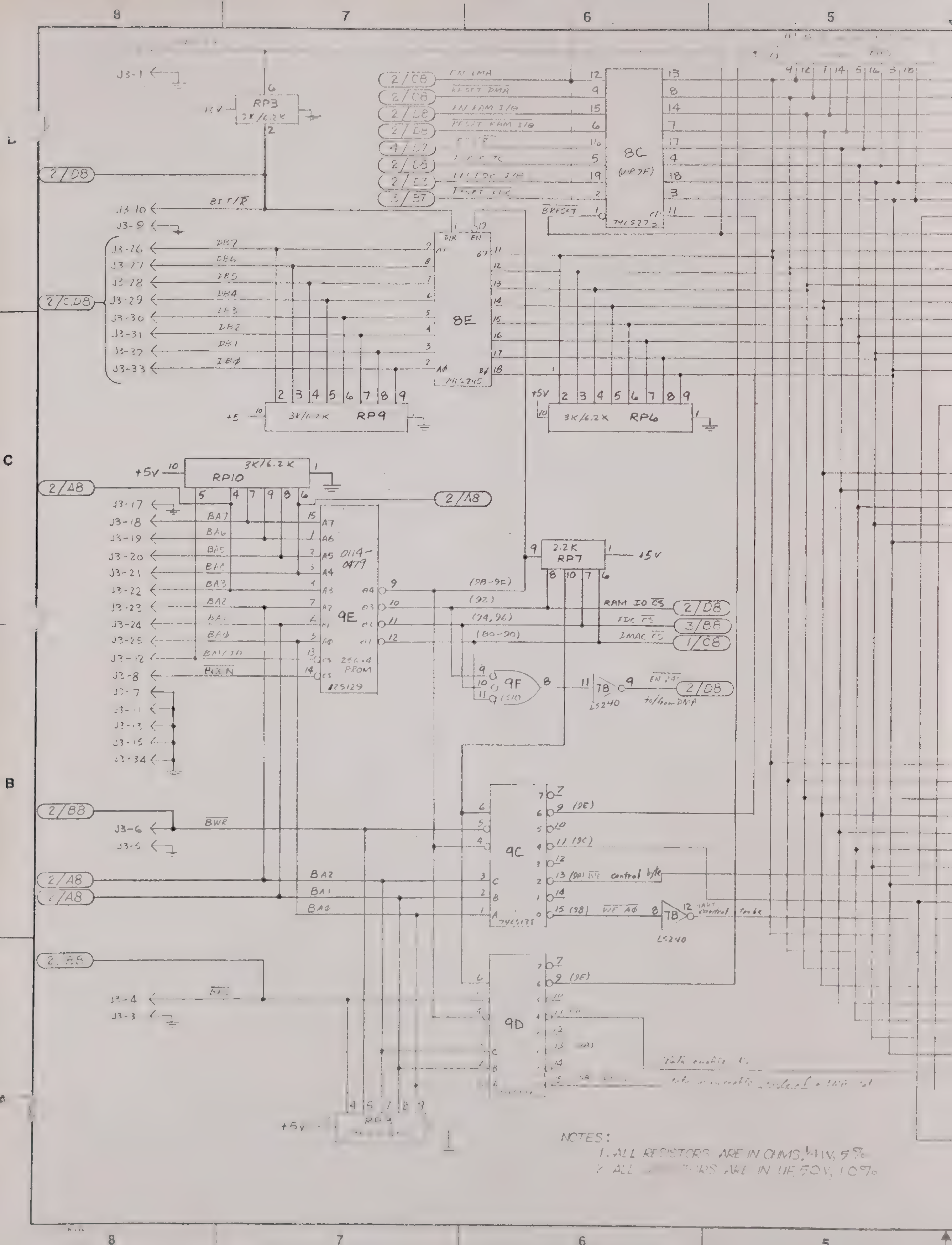
NOTES

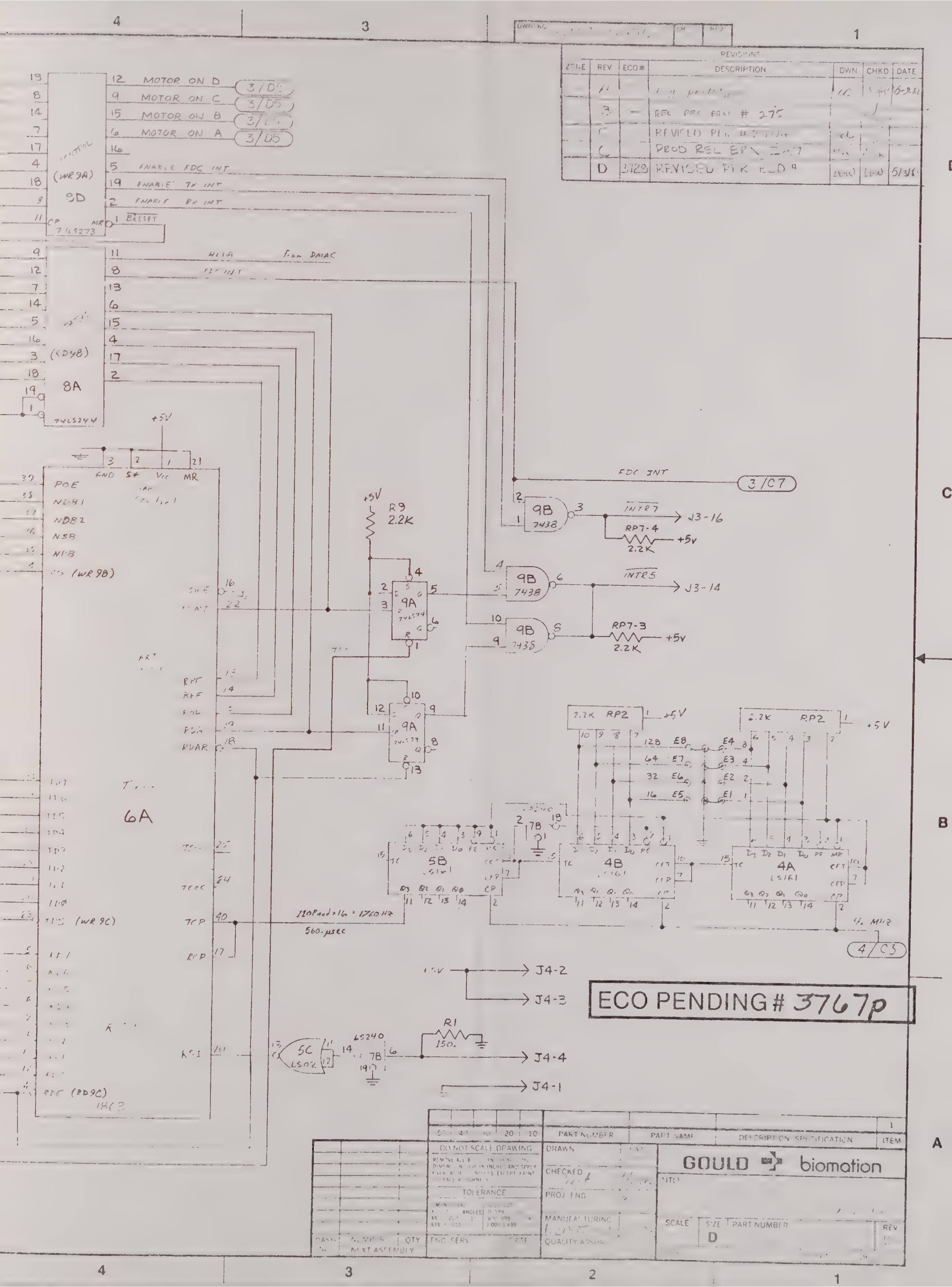
...TION	REFERENCE DESIGNATION	U/M
	for VR 1	

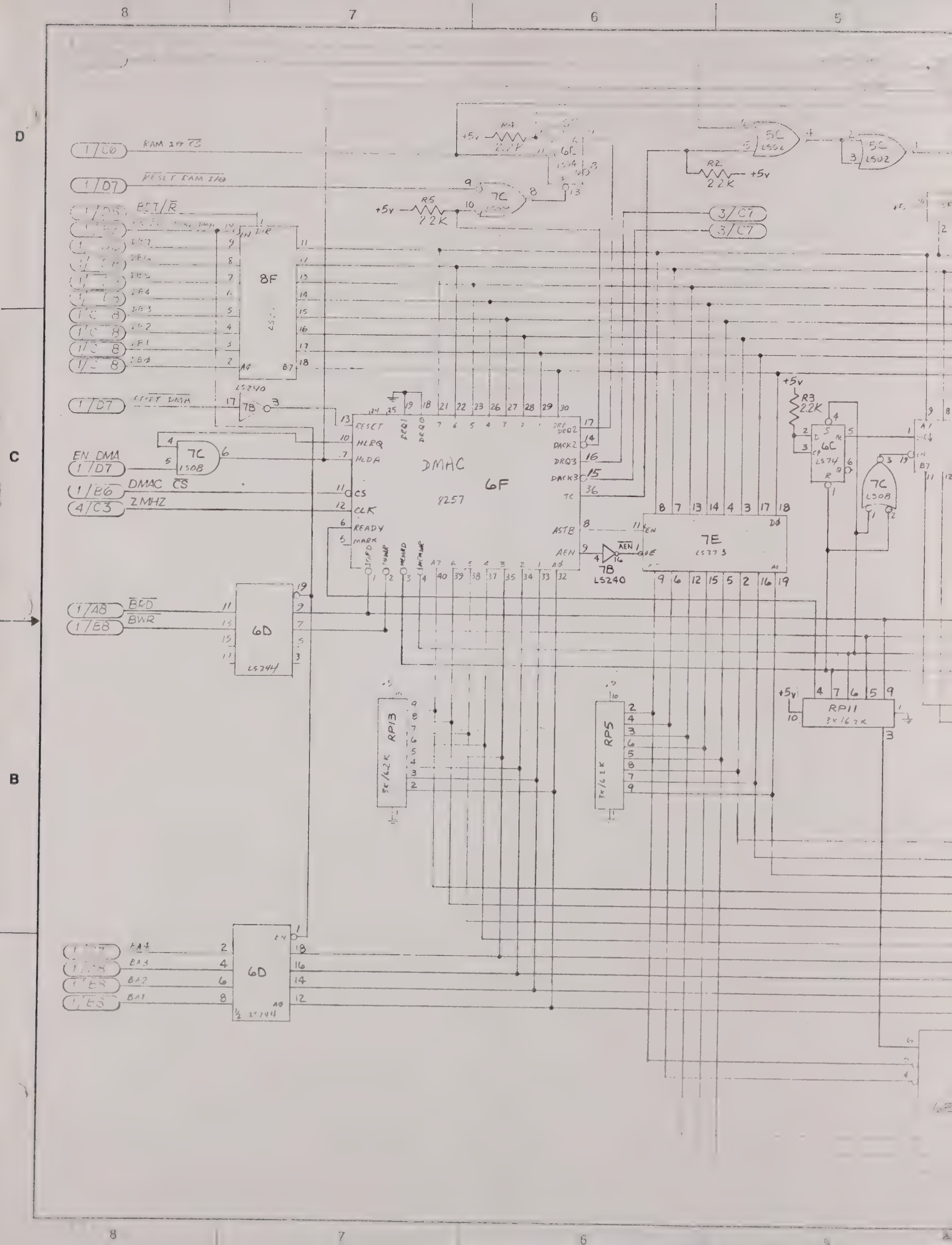
LIST OF MATERIAL

GOULD biomation

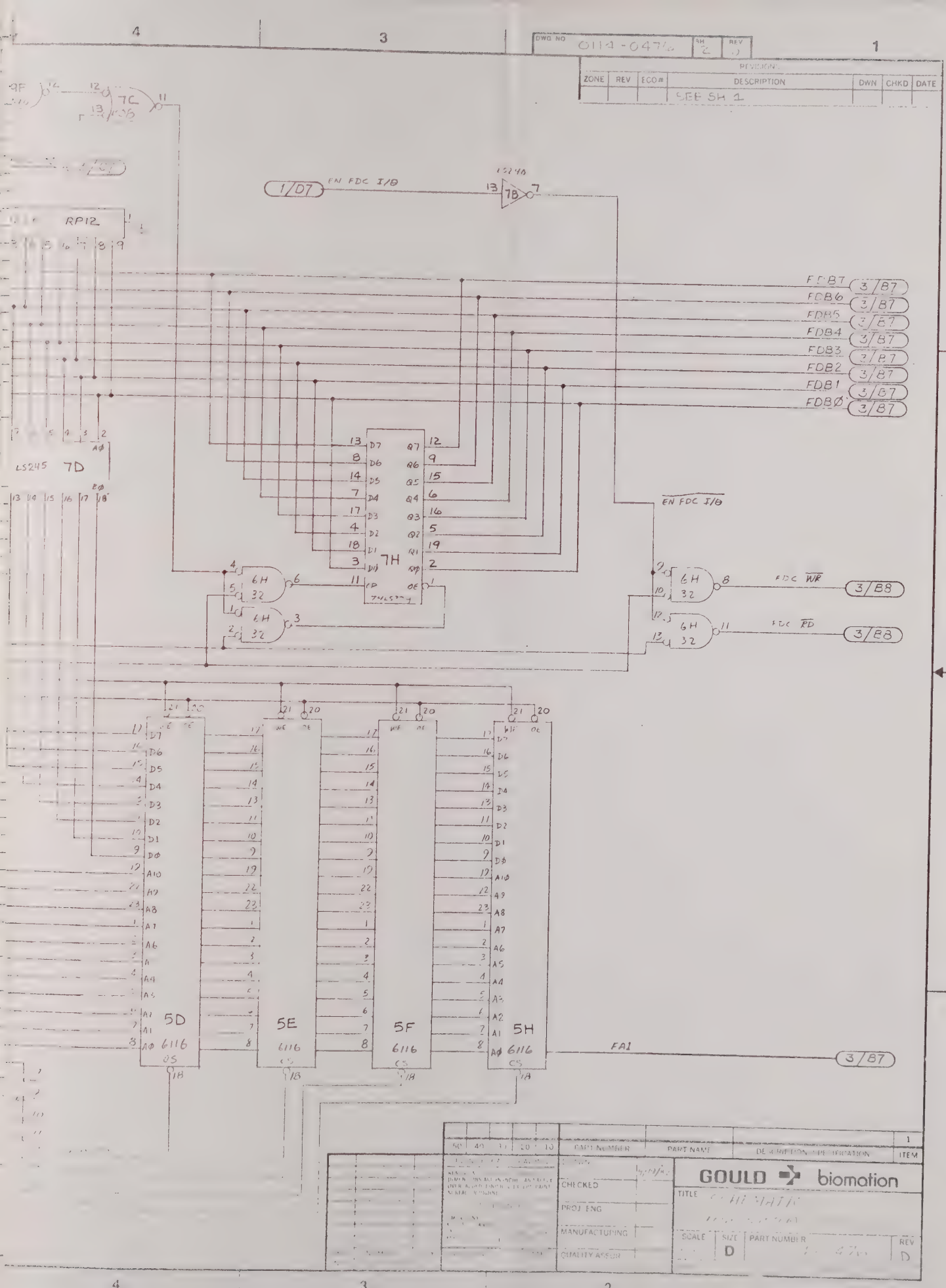
B	0114-0475	REV
MODEL	SHEET 3 OF 3	

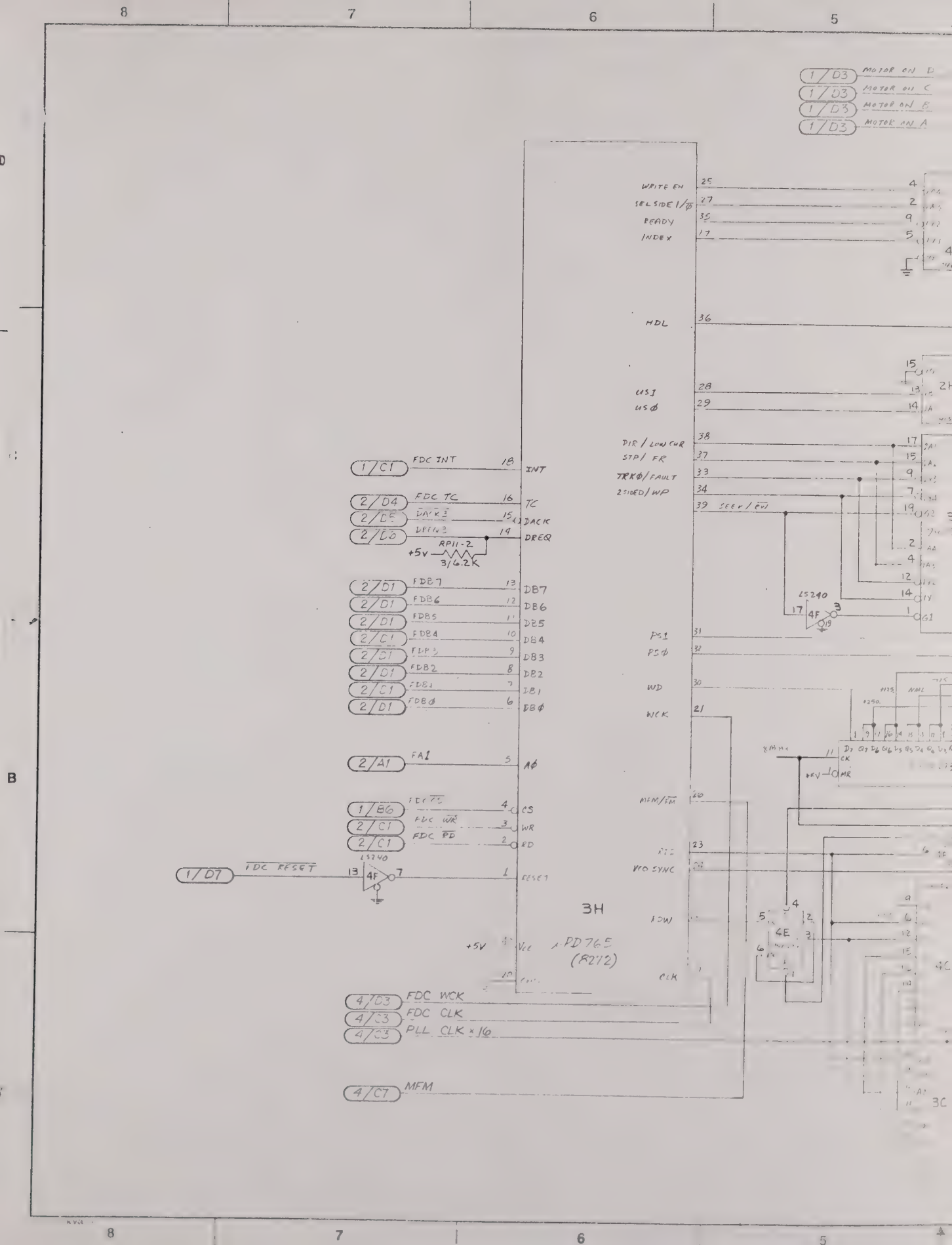

8
7
6
5
J3-1
RP3
3K/6.2K
2/D8
J3-10
BIT/R
J3-9
2/C8
EN DMA
RESET DMA
EN RAM I/O
RESET RAM I/O
8C
74LS273
2/C8
J3-26
DB7
J3-27
DB6
J3-28
DB5
J3-29
DB4
J3-30
DB3
J3-31
DB2
J3-32
DB1
J3-33
DBØ
DIR
EN
8E
74LS245
3K/6.2K
RP9
+5
+5V
3K/6.2K
RP6
C
+5V
RP10
3K/6.2K
2/A8
2/A8
J3-17
J3-18
BA7
J3-19
BA6
J3-20
BA5
J3-21
BA4
J3-22
BA3
J3-23
BA2
J3-24
BA1
J3-25
BAØ
J3-12
BA I/O
J3-8
BOON
J3-7
J3-11
J3-13
J3-15
J3-34
0114-0479
9E
256x4
PROM
82S129
2.2K
RP7
+5V
(98-9F)
(92)
(94,96)
(80-90)
RAM IO CS
2/D8
FDC CS
3/B8
IMAC CS
1/C8
9F
7B
LS240
EN 245
2/D8
to/from DMA
B
2/B8
J3-6
BWR
J3-5
9C
74LS138
(9E)
(9C)
control byte
BA2
BA1
BAØ
2/A8
2/A8
(98)
WE AØ
7B
LS240
J3-4
J3-3
9D
(9E)
+5v
NOTES:
1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%
2. ALL CAPACITORS ARE IN UF 50V, 10%
8
7
6
5


REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
D
3129
REVISED PER ECO
5/31
MOTOR ON D
MOTOR ON C
MOTOR ON B
MOTOR ON A
3/D5
ENABLE FDC INT
ENABLE TX INT
ENABLE RX INT
RESET
(WR 9A)
9D
74LS273
(RD 9B)
8A
74LS244
+5V
GND
S4
Vcc
MR
POE
NDB1
NDB2
NSB
NPB
(WR 9B)
6A
(WR 9C)
(RD 9C)
TCP
RCP
RDAR
FDC INT
3/C7
9B
7438
INTR7
J3-16
RP7-4
2.2K
+5v
INTR5
J3-14
RP7-3
R9
2.2K
9A
74LS74
2.2K RP2
128 E8 E4
64 E7 E3
32 E6 E2
16 E5 E1
5B
LS161
7B
4B
LS161
4A
LS161
110 Baud × 16 = 1760 Hz
560 μsec
4 MHz
4/C3
J4-2
J4-3
ECO PENDING # 3767p
5C
LS02
LS240
R1
150
J4-4
J4-1
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
GOULD biomation
TITLE
SCALE
SIZE
D
PART NUMBER
REV
NEXT ASSEMBLY
QTY
A
B
C
1
2
3
4

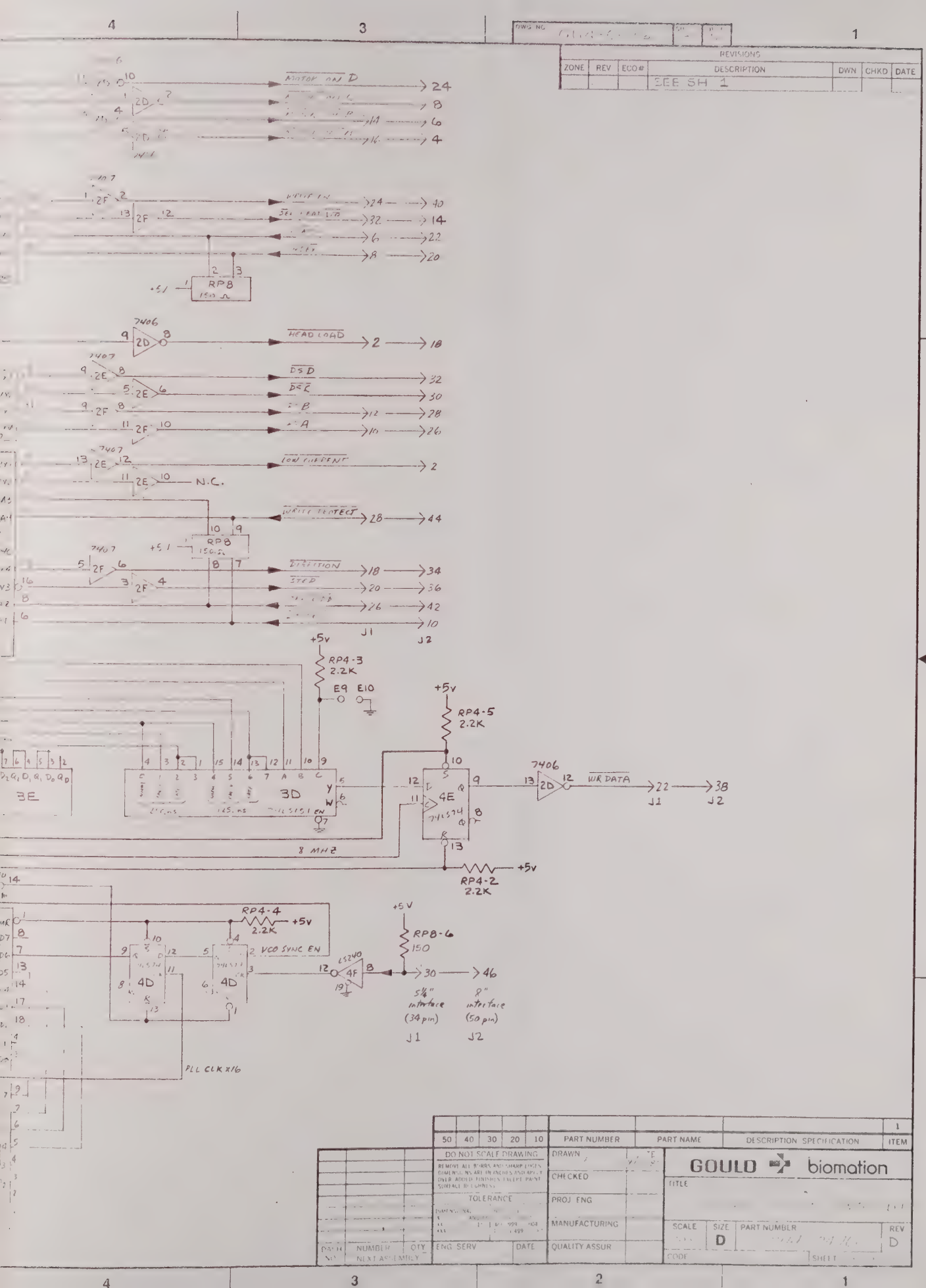


1/C6
1/D7
RESET RAM I/O
+5v
R4
R5
22K
R2
7C
6C
5C
LS02
3/C7
8F
LS240
1/D7
RESET DMA
7B
EN DMA
1/D7
LS08
1/B6
DMAC CS
4/C3
2MHZ
RESET
HLRQ
HLDA
CS
CLK
READY
MARK
DMAC
6F
8257
DRQ2
DACK2
DRQ3
DACK3
TC
ASTB
AEN
LS240
7E
LS373
+5v
R3
2.2K
6C
LS74
7C
LS08
1/A8
BRD
1/E8
BWR
6D
LS244
RP13
3x/6.2K
RP5
3x/6.2K
RP11
BA4
BA3
BA2
BA1
6D
1/2 LS244


DWG NO 0114-0476
SH 2
REV D
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SH 1
7C
RP12
1/D7
EN FDC I/O
LS240
7B
FDB7
FDB6
FDB5
FDB4
FDB3
FDB2
FDB1
FDBØ
3/B7
LS245
7D
7H
6H
32
EN FDC I/O
FDC WR
FDC RD
3/B8
5D
5E
5F
5H
6116
CS
FA1
3/B7
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
SCALE
SIZE
D
PART NUMBER
REV
D



MOTOR ON D
MOTOR ON C
MOTOR ON B
MOTOR ON A
WRITE EN
SEL SIDE 1/Ø
READY
INDEX
HDL
US1
USØ
DIR / LOW CUR
STP / FR
TRKØ / FAULT
2 SIDED / WP
SEEK / EW
PS1
PSØ
WD
WCK
MFM/FM
VCO SYNC
FDW
CLK
FDC INT
FDC TC
DACK3
DREQ3
RP11-2
+5V
3/6.2K
FDB7
FDB6
FDB5
FDB4
FDB3
FDB2
FDB1
FDBØ
FA1
FDC CS
FDC WR
FDC RD
FDC RESET
INT
TC
DACK
DREQ
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
AØ
CS
WR
RD
RESET
VCC
3H
PD765
(8272)
FDC WCK
FDC CLK
PLL CLK x 16
MFM
LS240
4F
4E


REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SH 1
MOTOR ON D
HEAD LOAD
DS D
DS C
B
A
LOW CURRENT
N.C.
WRITE PROTECT
DIRECTION
STEP
RP8
150Ω
RP4-3
2.2K
RP4-5
2.2K
RP4-2
2.2K
RP4-4
2.2K
RP8-6
150
E9 E10
+5V
7406
WR DATA
8 MHZ
VCO SYNC EN
PLL CLK X16
5¼" interface (34 pin)
8" interface (50 pin)
J1
J2
3E
3D
4E
4D
4F
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
DRAWN
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PROJ ENG
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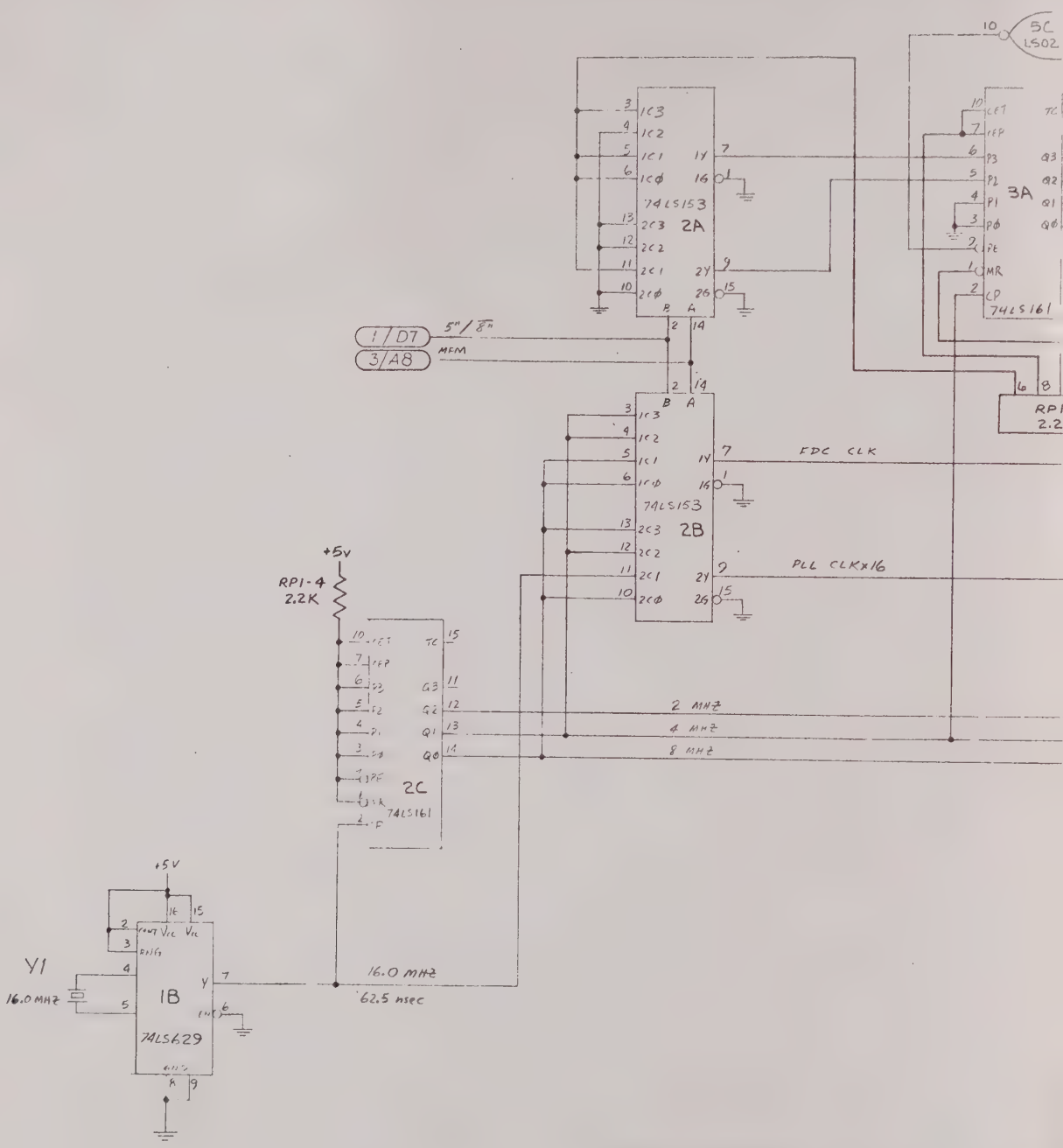
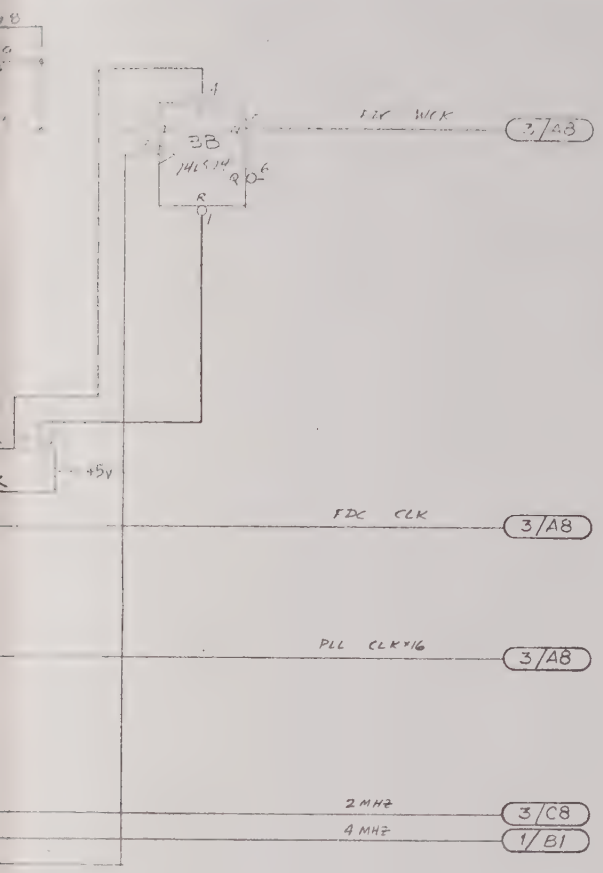
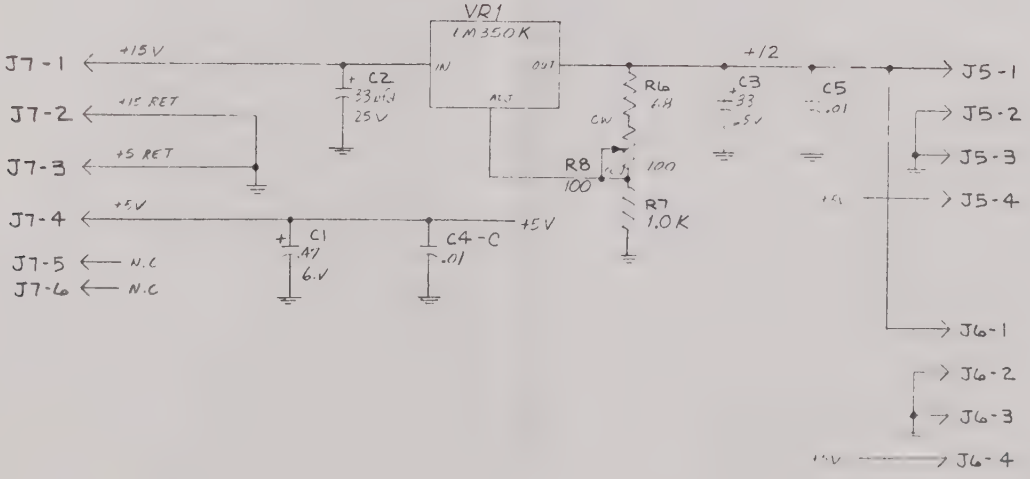
QUALITY ASSUR
ENG SERV
DATE
GOULD biomation
TITLE
SCALE
SIZE D
PART NUMBER
REV D
CODE
SHEET



5"	MEM	DESCRIPTION	FDC CLK	PLL CLKx16	FDC WCK
0	0	8" SINGLE DENSITY	8 MHZ	8 MHZ	500 KHZ
0	1	8" DOUBLE DENSITY	8 MHZ	16 MHZ	1 MHZ
1	0	5" SINGLE DENSITY	4 MHZ	4 MHZ	250 KHZ
1	1	5" DOUBLE DENSITY	4 MHZ	8 MHZ	500 KHZ

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH 1			





50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

DRAWN DATE

CHECKED

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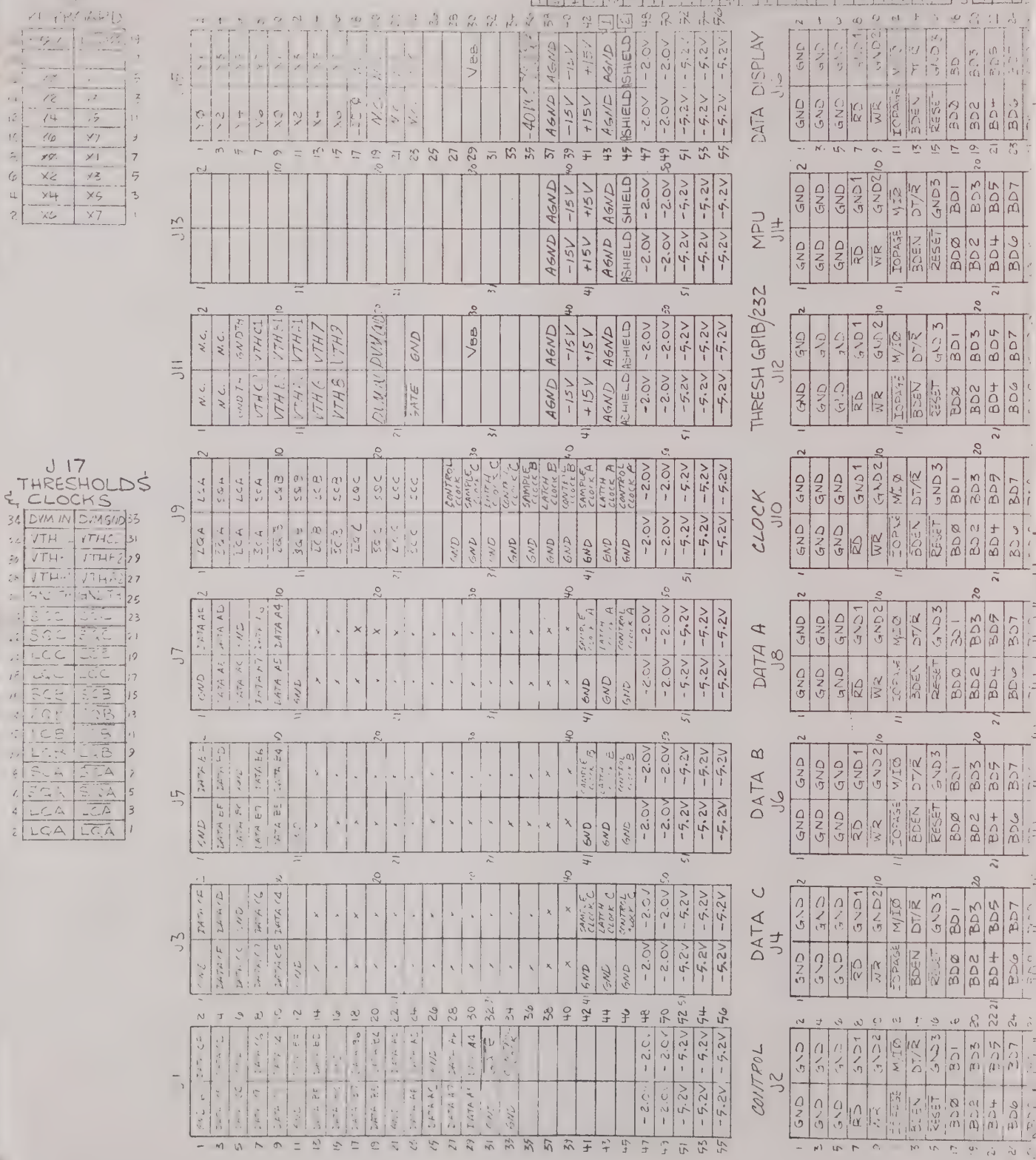
QUALITY ASSUR

GOULD biomation

SCALE SIZE PART NUMBER

D



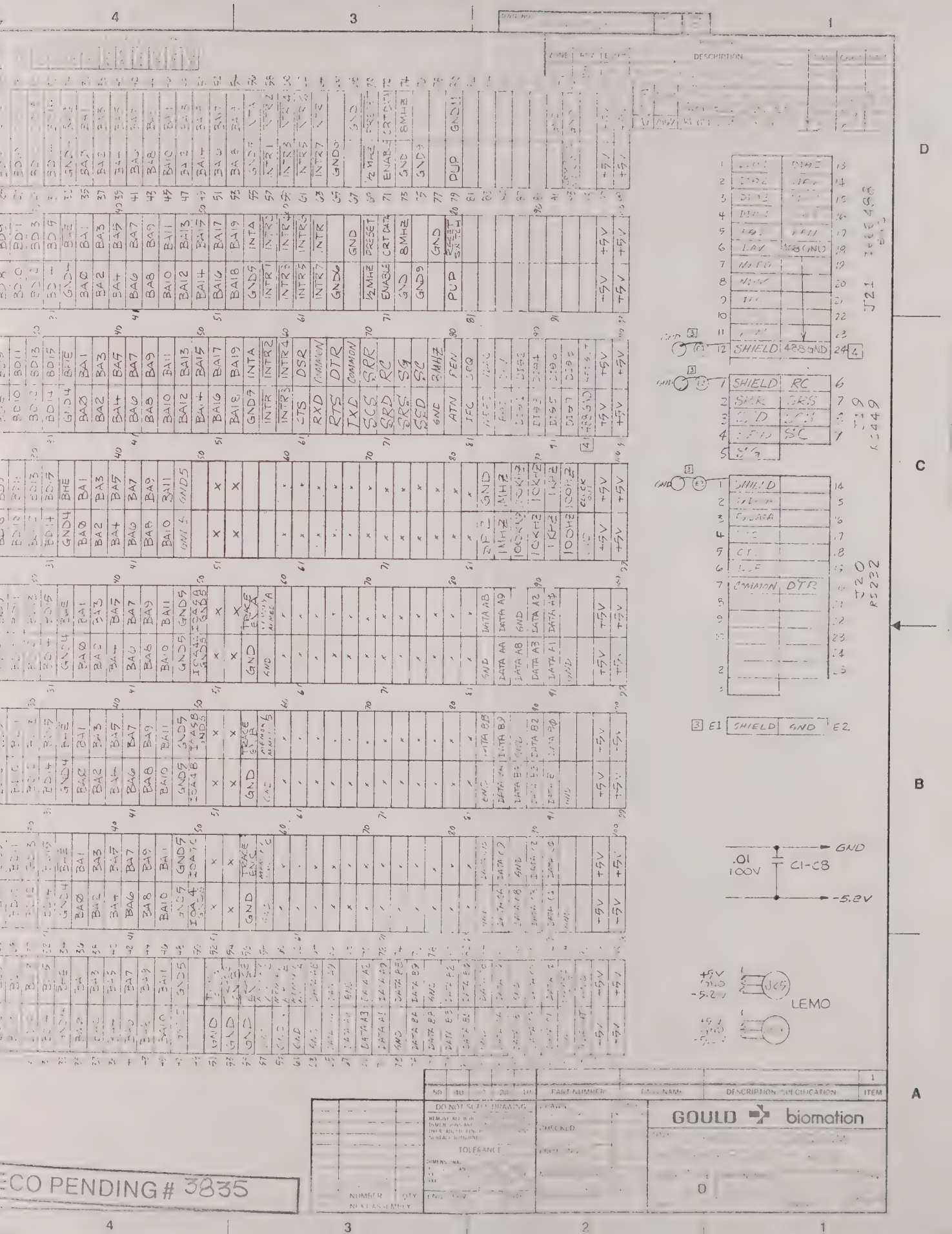
NOTES:

AGND IS CONNECTED TO GND AT PINS J22-2,12.

ASHIELD IS CONNECTED TO GND AT PIN [illegible]-14

[illegible] CONNECTED [illegible] E1(488), E2(449), E3(232)

[illegible] CONNECTED [illegible]



DESCRIPTION
J21
J19
RS449
J20
RS232
SHIELD
488GND
RC
SRS
SC
COMMON
DTR
E1
E2
GND
.01
100V
C1-C8
-5.2V
LEMO
PART NUMBER
DESCRIPTION SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
ECO PENDING # 3835

COMMENTS		TOTAL COST	UNIT COST
-10 AID KEYBOARD			
-20 KIDDTYPE KEYBD.			
-30 - VOID -			
-40 NEW DISPLAY ED. (STORAGE SYS)			

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
1			1		1	1	011
2			1		—	1	011
3			1		1	1	0114-
4			1		1	1	0114
5			1		1	1	011
6			3		3	3	011
7			1		1	1	0114
8			1		1	1	0114
9			1		—	—	0114-
10			1		1	1	0114-
11			—		1	1	0114-
12			1		1	1	0114
13			1		1	1	0114
14			10		12	12	700
15			2		2	2	700
16			2		2	2	—
17			1		1	1	095
18			2		2	2	011

DASH NO.	NUMBER	QTY
-20	0114-0001-20	1
-10	0114-0001-10	1
	NEXT ASSEMBLY	

DRAWN J. PERGIA
CHECKED RG
ENGINEER
MANUFACTURIN
QUALITY ASSUR

RT NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]-0003	CHASSIS ASSY				[illegible]
[illegible]10	BEZEL ASSY			AND [illegible]	[illegible]
0039-10	COVER, TOP				
-0039-20	COVER, BOTTOM				
-0016	HANDLE ASSY				LM
-0110	H.S. DATA PWB ASSY (10422)				LM
-0120-10	RECORD CONTROL PWB ASSY (10422)				LM
-0160	CLOCK PWB ASSY				LM
2010-20	DATA DISPLAY PWB ASSY				LM
0170-20	GPIB/RS232 PWB ASSY				LM
0185-20	MPU PWB ASSY				LM
-0049	CARD RETAINER BKT				
-0054	CABLE, CONTROL Bd TO CLOCK Bd				LM
7-0368	SCREW			#6-32 x 3/8" LG 100° FLT HEAD	
0-0376	SOC. HD CAP SCR.			1/4"-20 x 3/4" LG	
———	WASHER			1/4" SPLIT LOCK, HEL.	
0-0142	CRT CABLE ASSY				LM
-0059	BAIL, KNOB				

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PILOT REL ERN # 0103	2/4/81	JKP	RG	
	B	REVISED PER ECO # 1871	8-1-8[illegible]	JWC	RD	
	C	REVISED PER ECO 1888	[illegible]	[illegible]	RD	
	D	REVISED PER ECO 1877	[illegible]	[illegible]	[illegible]	
	D	REL TO PROD ERN # 203	[illegible]	[illegible]	[illegible]	
	E	REVISED PER ECO # 2188	11/4[illegible]	[illegible]	[illegible]	
	F	REVISED PER ECO # [illegible]	[illegible]	[illegible]	TJ	

	DATE
[illegible]	2/4/81
	[illegible]
	10-R-81
[illegible]	[illegible]
[illegible]	

LIST OF MATERIAL

TOP ASSEMBLY

biomation

B	0114-0002	REV J

MODEL

CODE K101

SHEET 1 OF 2

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PAR
	-60	-50	-40	-30	-20	-10	
19							
20			1		1	1	CAP
21			1		1	1	7300
22			REF		—	—	TOP STDA
23			—		1	—	0114-
24			—		1	1	0114-
25			1		1	1	0114-
26							
27			1		—	—	0114-C

			RE

			DRAWN J. PERG
			CHECKED
			ENGINEER
			MANUFACTURING
			QUALITY ASSURAI
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
[illegible]	CARD RETAINER				
-0019	FUSE			7A (125V)	
[illegible]					LM
0005-20	BEZEL ASSY			BIOMATION KEY BD	LM
0130-20	DATA BD.				
-0081	RETAINER CLIP PROBE TEST CONN				
185-40	MPU PWB Bd.				LM

F. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	REVISED PER ECO 2654	12-9-82	DGW		
	H	REVISED PER ECO 2765A	[illegible]	[illegible]	[illegible]	[illegible]
	J	REVISED PER ECO 3682	[illegible]	[illegible]	DGW	[illegible]

	DATE
[illegible]	2/1/81
NCE	

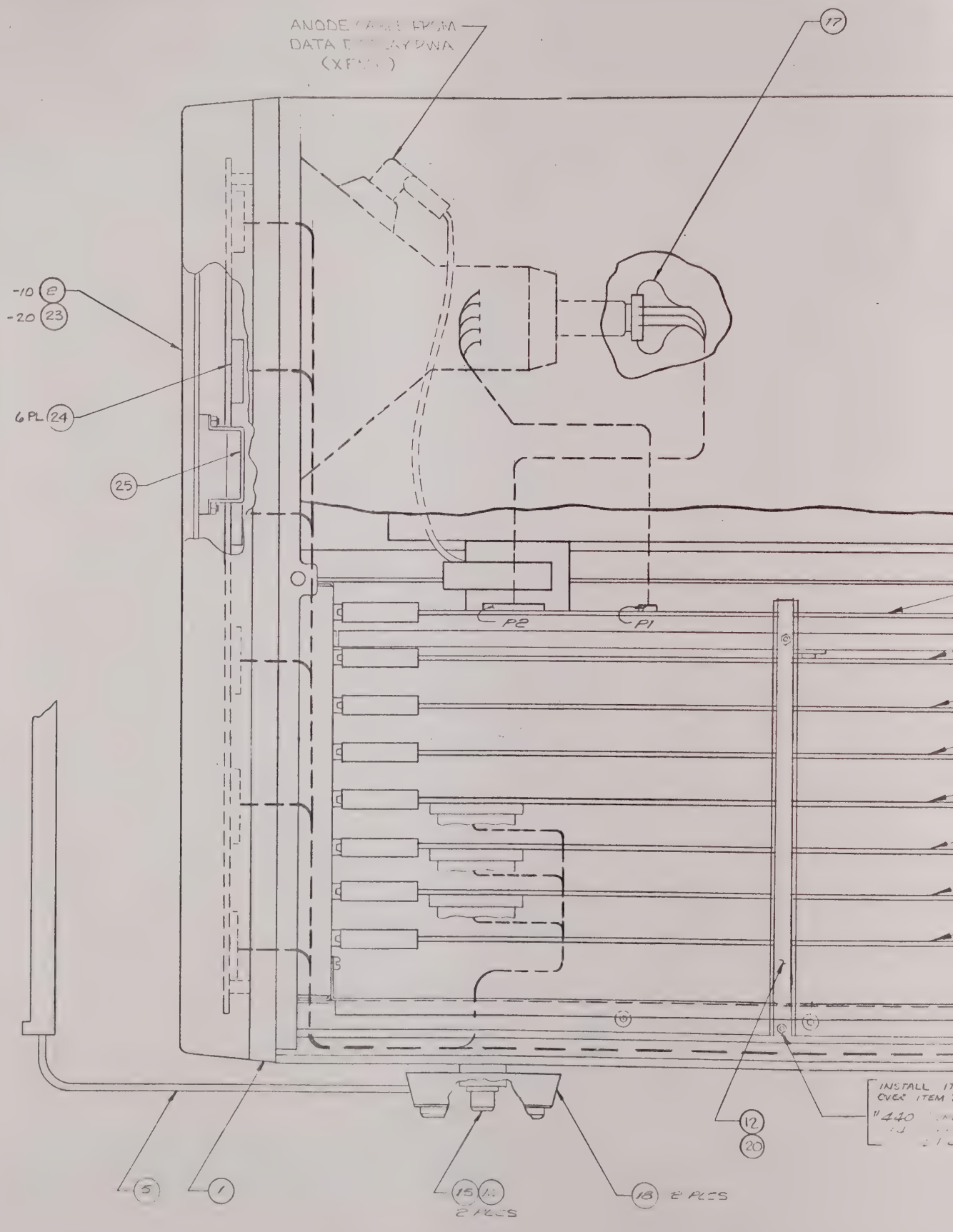
LIST OF MATERIAL

TOP ASSEMBLY

biomation

B	0114-0302	REV J

MODEL | CODE [illegible] | SHEET [illegible] OF [illegible]


ANODE CABLE FROM
DATA DISPLAY PWA
(XP1)
17
-10 E
-20 23
6 PL 24
25
P2
P1
INSTALL
OVER ITEM
12
20
5
1
15
2 PLCS
18
2 PLCS

DWG NO 0111-0006 SH 1 REV

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER ERN 103	JKP		
	B	1871	REVISED PER ECO	JWC	[illegible]	[illegible]
	C	1889	REVISED PER ECO #	JWC	[illegible]	2-6-81
	D	1977	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	E	—	PROD REL ERN # 203	[illegible]	KC	[illegible]
	E	2188	REVISED PER ECO.	MC	[illegible]	10/6/82
	F	2349	REVISED PER ECO NO	JWC	TJ	3-3-83
	G	2465A	REVISED PER ECO N#	DLW	[illegible]	[illegible]
	H	2705A	REVISED PER ECO N#	MW	DLW	2-14-84
	J	3682	REVISED PER ECO	MW	DLW	5/6/85

(4) (14) 12 PLCS (-10 -20)

(24) DATA DISPLAY PWB (-10 -20)
(9) DATA DISPLAY PWB ASSY (-40)
(27) MPU PWB ASSY (-40)
(11) MPU PWB ASSY (-10 -20)
(10) GPIB/RS232 PWB ASSY
(8) CLOCK PWB ASSY
(6) H.S DATA PWB ASSY
(6) H.S DATA PWB ASSY
(6) H.S DATA PWB ASSY
(7) RECORD CONTROL PWB ASSY

(13)

WITH

DESCRIPTION SPECIFICATION ITEM

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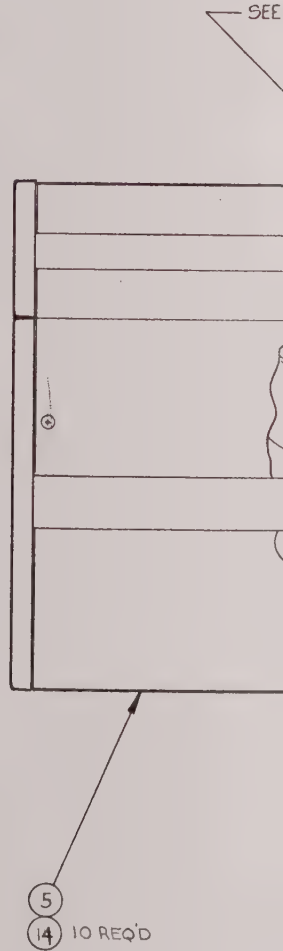
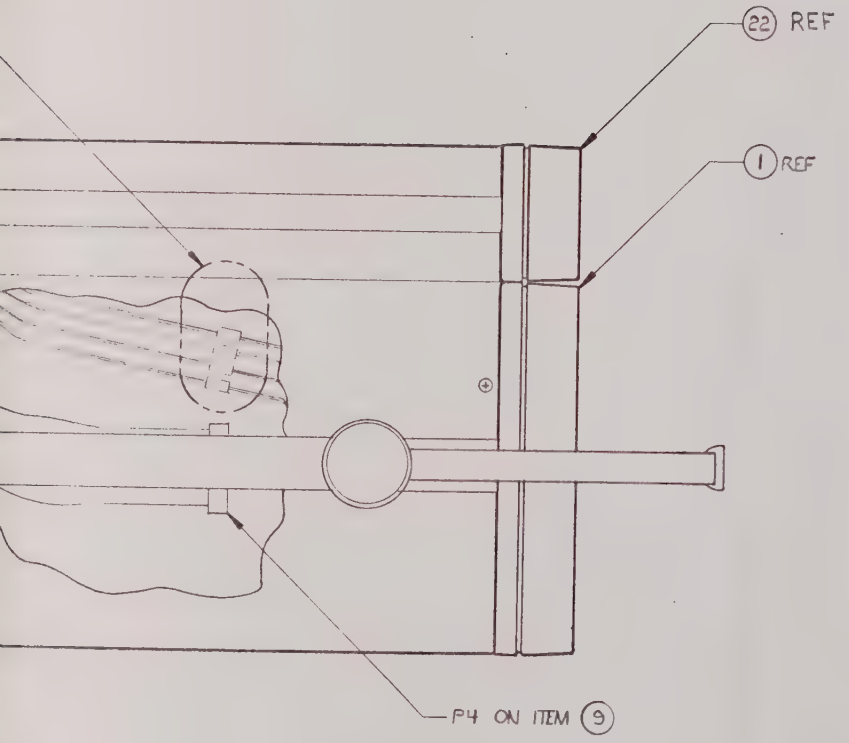
D

TAB. LATION			
STORAGE SYS PWR CABLE	COLOR	PWR SUPPLY CABLE TO MOTHERBOARD	DESCRIPTION
J7 – 1	WHT	J22 – 3	+ 15 V
J7 – 2	BLK	J22 – 2	GND
J7 – 3	BLK	J23 – 10	GND
J7 – 4	RED	J23 – 9	+ 5V



ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

TABULATION



-40 ONLY

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

DRAWN

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TITLE

TOP ASSY

SCALE 1:2 | SIZE D | PART NUMBER [illegible] | REV J

CODE [illegible] | SHEET [illegible] OF

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
1						1	011
2							
3							
4						2	011
5							
6							
7						14	400
8							
9						5	600
10						4	600
11							
12						3	600
13							
14						4	600
15							
16						1	600
17						1	600
18						1	600

ASSEMBLY TIME

COMPONENT LEAD SPACING

CAPS .15

ECO PENDING # 383

-10	0114-0001	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

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QUALITY ASSUR

T [illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0212	PWB				FAB
[illegible]	SUPPORT BAR				[illegible]
0-0025	CAPACITOR	C1-14		.1uf 50V	
-0198	CONNECTOR	J1, 9, 11, 13, 15		28 PIN DUAL	
0-[illegible]	CONNECTOR	J2, 12, 14, 16		50 PIN DUAL	
-0369	CONNECTOR	J3, 5, 7		28 PIN DUAL W/ SELECT INSERTION	
-0370	CONNECTOR	J4, 6, 8, 10		50 PIN DUAL W/ SELECT INSERTION	
-0335-22	CONN, HDR	J22		22 PIN ST NON LCK	
-0335	HEADER	J23		10 POS	
0-[illegible]	CONN, HDR	J24		3 PIN, ST NON LCK	

EF Drawings	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PROTO	2-6-81	[illegible]		
	B	PRE PILOT REL ERN #101			[illegible]	
	C	REVISED PER ECO 1715	5-8-8[illegible]	JL	[illegible]	
	C	PROD REL PER ERN #0207	[illegible]	[illegible]	[illegible]	
	D	REVISED PER ECO #2462	3/24/82	[illegible]	[illegible]	
	E	NOT INCOR[illegible]	[illegible]	[illegible]		
	F	REVISED PER ECO 3585 A	[illegible]	[illegible]	[illegible]	

	DATE
[illegible]	[illegible]
[illegible]	4/5/82
[illegible]	1-7-82
[illegible]	1/7/82
[illegible]	

LIST OF MATERIAL

ASSY—

MOTHER PWB K101D

biomation

B | 0114-0210 | REV F

MODEL | CODE | SHEET 1 OF [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PA
	-60	-50	-40	-30	-20	-10	
19						1	6000
20						1	600
21							
22							
23						1	600
24							
25						1	600
26							
27						1	600
28							
29						1	7000
30						2	700
31							
32							
33						4	900
34							
35							
36							

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	Burt
CHECKED	
ENGINEER	
MANUFACTURIN	
QUALITY ASSUR	

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
-0373	HEADER, RT. ANGLE	J17		34 PIN W/EARS	
		J18		20 PIN W/EARS	
-0315	RECEPTACLE	J21		24 POS. RT ANGLE (FOR IEEE 488)	
-0353	RECEPTACLE	J20		25 POS. RT. ANGLE (FOR RS232)	
-0388	RECEPTACLE	J19		9 POS. RT. ANGLE (FOR RS449)	
-0399	KIT, MTG. HDWRE	@ J21			
-0425	KIT, MTG HDWRE	@ J19, J20			
-0054	BUSS WIRE	TP1-4			

EF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE
E.	2-6-81
	1.7.81
ANCE	

LIST OF MATERIAL

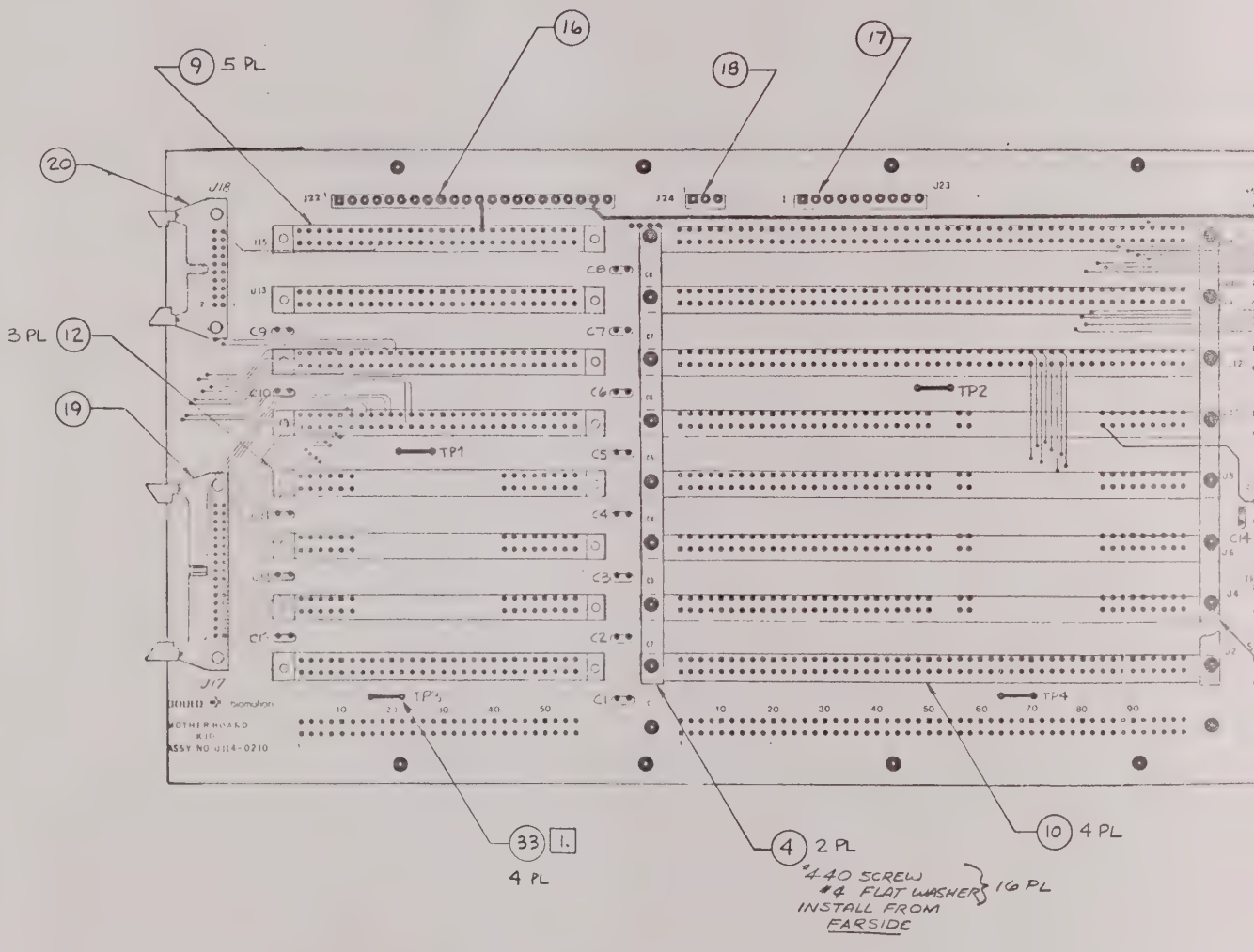
ASSY—

MOTHER PWB. K101D

biomation

B | 0114-0210 | REV E

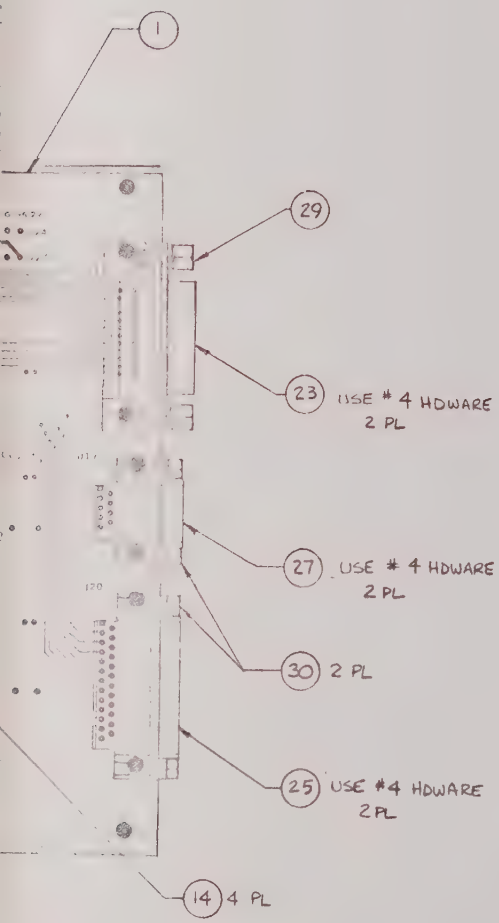
MODEL K101 | CODE | SHEET 2 OF 2



NOTES:

1. INSTALL GND BUSS WIRE; ITEM 33; ON FARSIDE AT TP1-4.

			DESCRIPTION			
			[illegible]			
			[illegible]			
			PROD REL PER ERN			
			REVISED PER [illegible]			
			[illegible]			
	F		REVISED PER ECO			



ECO PENDING # 3835

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION	ITEM

GOULD biomation

TITLE ASSEMBLY — MOTHER [illegible], KIOID

SCALE D PART NUMBER 0114-

CHECKED

PROJ ENG

NUMBER | QTY | ENG SIZE

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						PAR
	-60	-50	-40	-30	-20	-10	
1						1	0114
2							
3							
4						56	
5						1	0114
6							
7							
8							
9							
10							

			DRAWN S.R.
			CHECKED
			ENGINEER
			MANUFACTURIN
			QUALITY ASSUR
-10	[illegible]	1	
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

T NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
-0202	PWB			SNAP DOME	
— ,	SNAP SWITCH		9100-004-001	A.I.D.	
-0050	CABLE ASSY				

F. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	B	REL PER ERN 0121	2-11-80	[illegible]	RD	

	DATE
ELL	2-11-80
NCE	

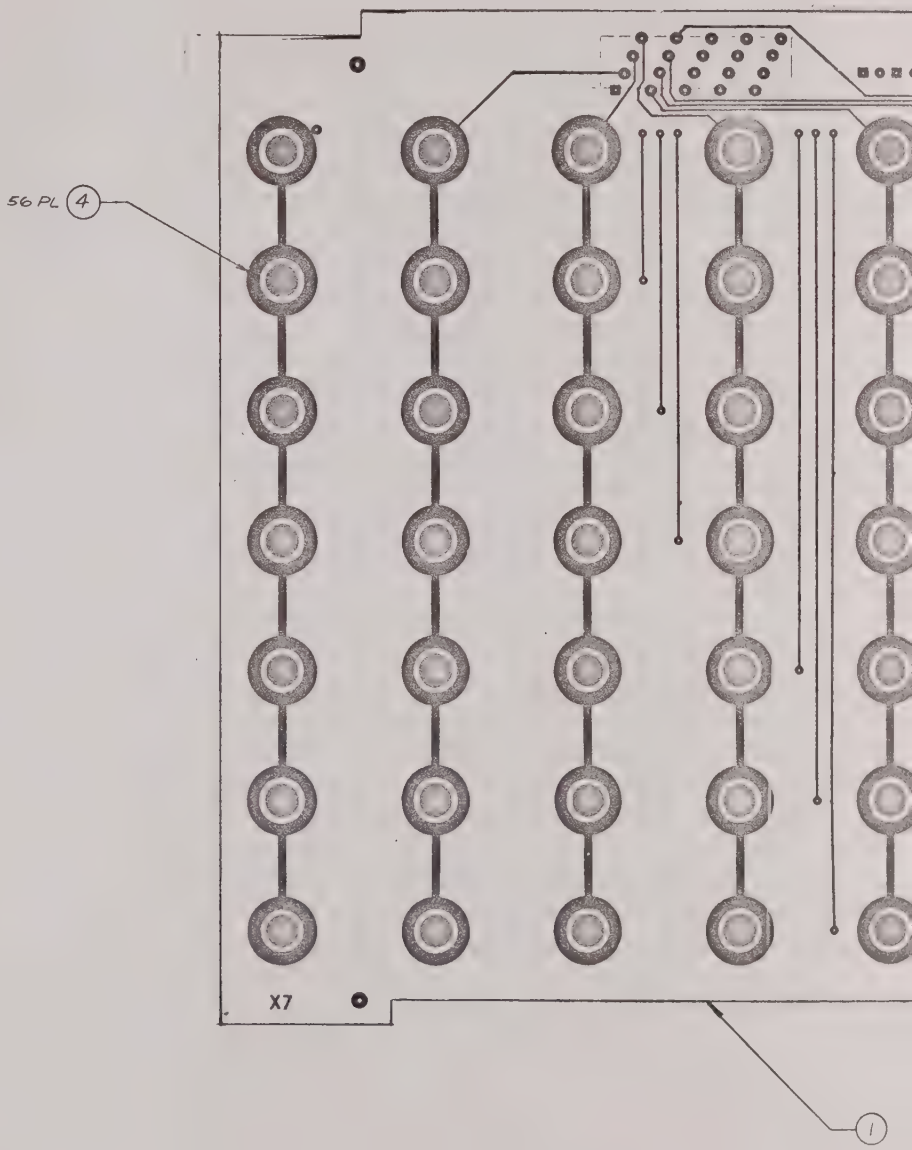
LIST OF MATERIAL

ASSEMBLY,
K101 SNAP-DOME KEYBOARD

biomation

B	0114-0200	REV B

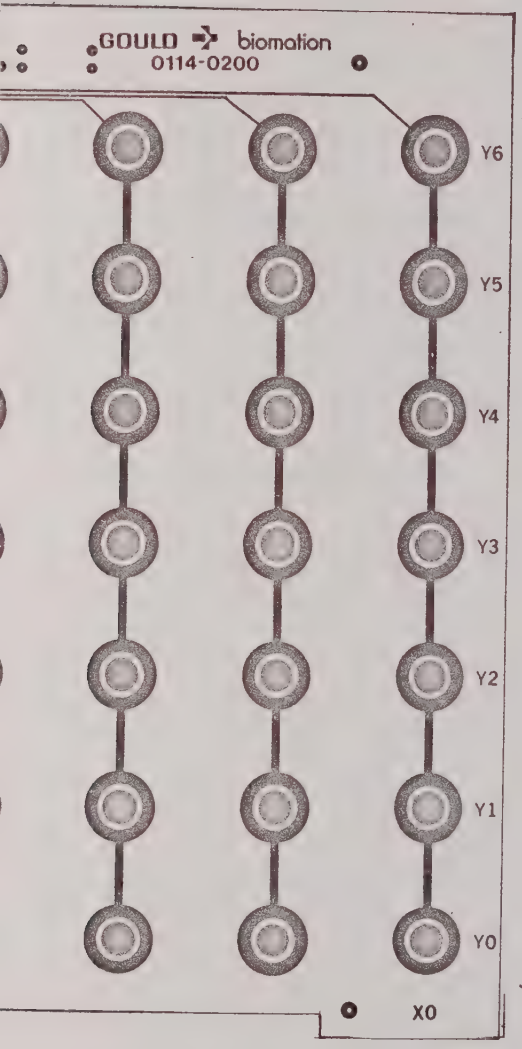
	MODEL	CODE	SHEET 1 OF 1

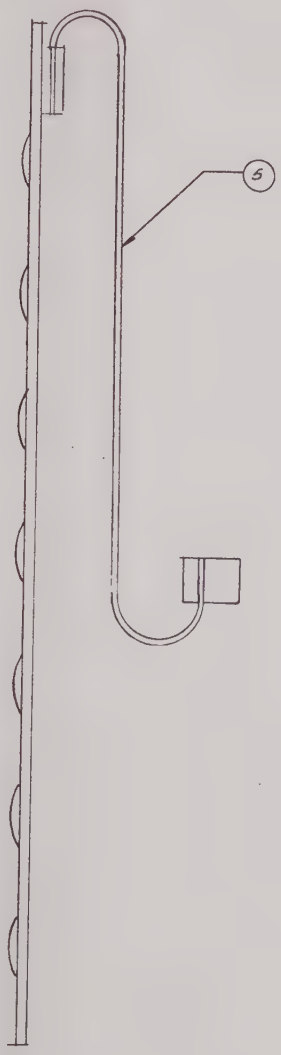

56 PL (4)
X7
(1)

DWG NO	SH	REV
[illegible]		

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		[illegible]			
	B		PLOT ALL [illegible]	[illegible]	[illegible]	





50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY ONLY ADDED FINISHES EXCEPT PAINT [illegible]

TOLERANCE

DIMENSIONAL [illegible]

DASH NO	NUMBER NEXT ASSEMBLY	QTY

ENG SERV | DATE

DRAWN	DATE
CHECKED	
PROJ ENG	
MANUFACTURING	
QUALITY ASSUR	

GOULD biomation

TITLE [illegible]

K101 SNAP-DOME KEYBOARD

SCALE	SIZE	PART NUMBER	REV
	D	[illegible]	[illegible]

CODE | SHEET | OF

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